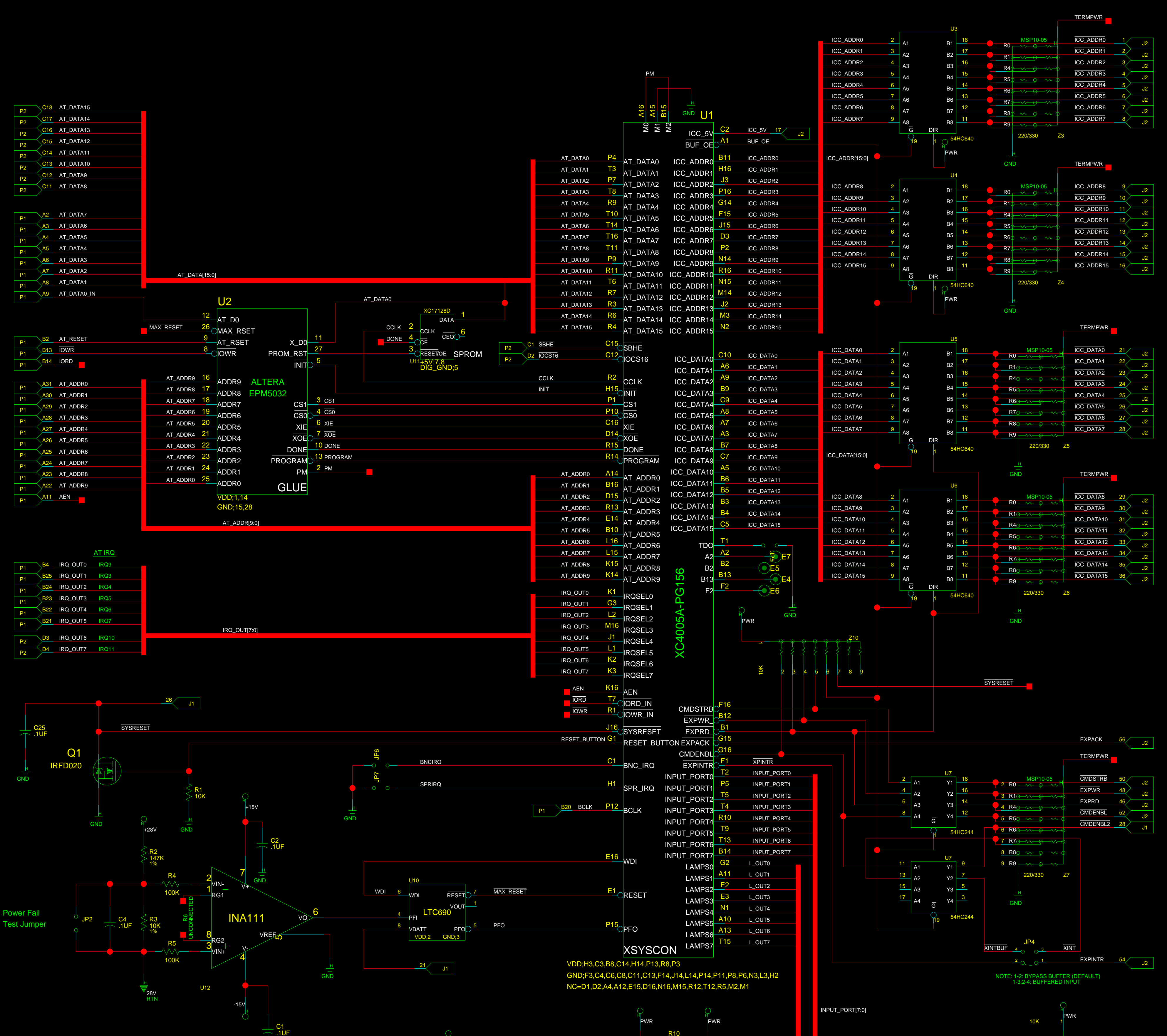
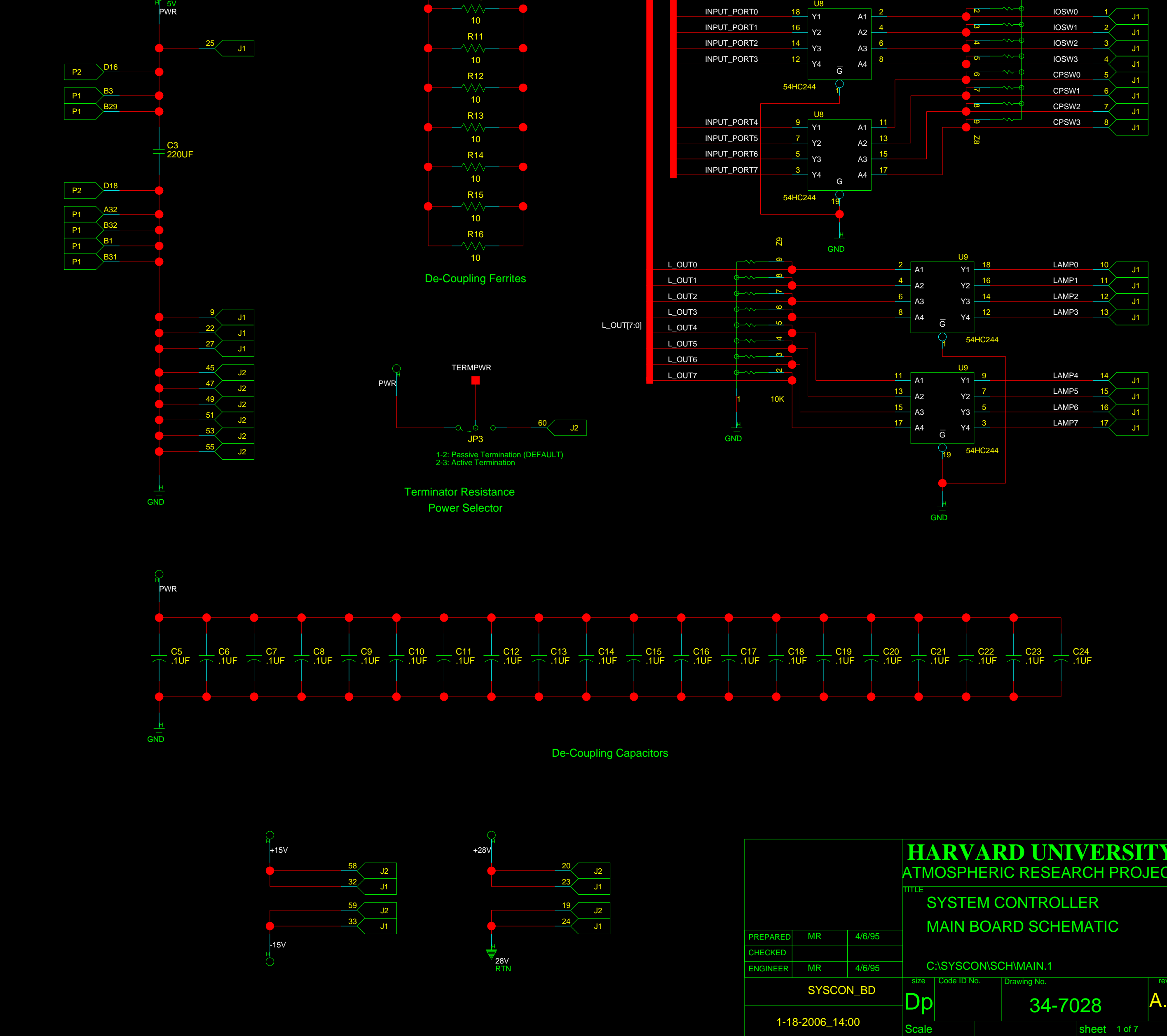


Revisions				
Zone	Iter	Description	Date	Approved
A.1.2		Initial Rel w/ Notes, Mods	4/6/95	
A.1.3		U2 (glue) substitution	2/8/97	



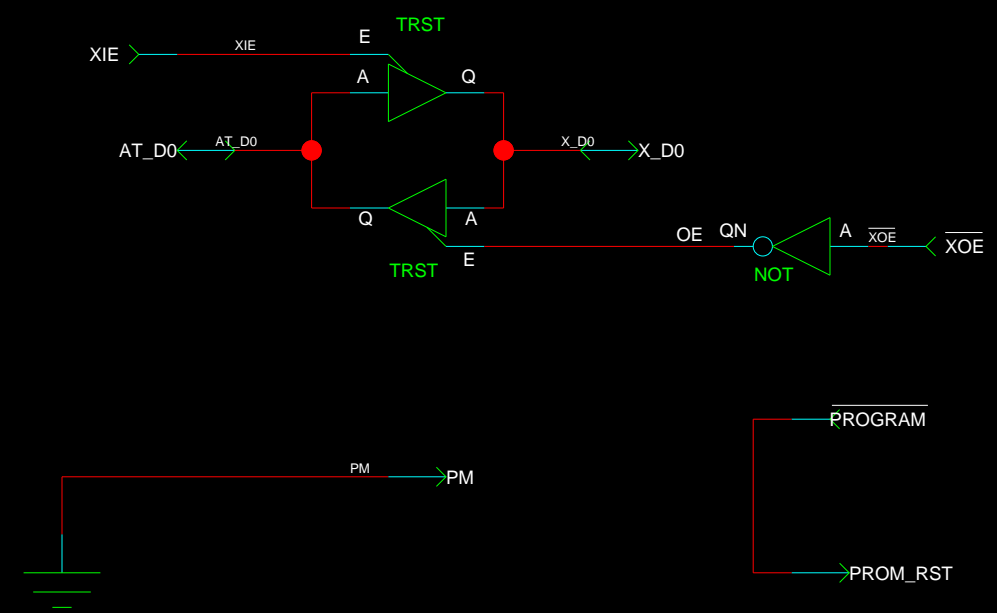
- ASSEMBLY NOTES:**
- Ferrite beads are inserted between (5 Volts and the Vdd pin) of all 54HC/HCT parts. (Implemented on Printed Circuit Board)
 - P1, P2, J2: Elevated Stackthrough EURO-style .100" Connectors (PC/104)
 - J1: EURO-Style .100" unshrouded header. 34 pins
 - All bypass caps 0.1uF
 - Jumpers installed as shown
- BOARD MODIFICATIONS:**
- Connect J2.57-J1.31-J1.29-J1.27 (AnaGnd-DigGnd)
 - Connect J1.21- J1.22 (VBatt-DigGnd)
 - Z7: Install 10K Pullup only Resistor Network (091 style)
 - If 101 style (10 pin), clip unused Z7.9 pin
 - Criss cross R4 and R5:
 - Connect R4.2-U12.3, and R5.2-U12.2
 - Connect 1K resistor from JP2.1 to J1.27,29,31 (Relate 28Vtrn to AnaGnd/DigGnd)
 - Connect J2.37-JP7.1
- Rev: A.1.2

- GLUE-Bypass Modifications:**
- Connect U2.13-U2.27 (PROG1-RESET)
 - Connect U2.12-U2.4 (DO)
 - Connect U2.2-U2.28 (PM-GND)
 - Pullup: Connect U2.13/U2.27-Z10.8 (PROG1)
 - Pullup: Connect U2.10-Z10.9 (DONE)
 - Optional Jumper between U2.2-U2.3
- Rev: A.1.3

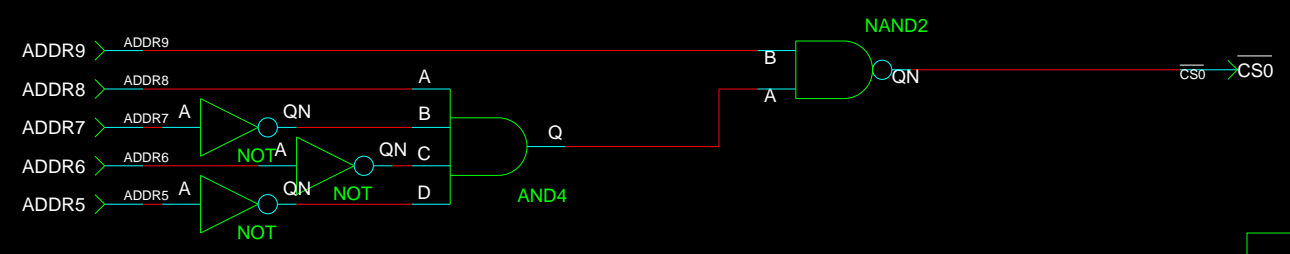


HARVARD UNIVERSITY			
ATMOSPHERIC RESEARCH PROJECT			
TITLE			
SYSTEM CONTROLLER			
MAIN BOARD SCHEMATIC			
PREPARED	MR	4/6/95	
CHECKED	MR	4/6/95	
ENGINEER	MR	4/6/95	
SYSCON_BD		size	Code ID No.
Dp		34-7028	A.1
1-18-2006-14:00		Scale	Sheet 1 of 7

Revisions				
Zone	Itr	Description	Date	Approved



Active LOW PROM RESET



PREPARED	MR	
CHECKED		
ENGINEER	MR	

HARVARD UNIVERSITY
 ATMOSPHERIC RESEARCH PROJECT
 TITLE
LTWT SYSTEM CONTROLLER
GLUE LOGIC

BSHEET
 10-2-2002_11:40

size	Code ID No.	Drawing No.	rev
B		x23_7028	A
Scale	NO	APR[21]-95	sheet 14 of 41

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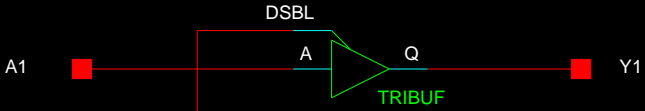
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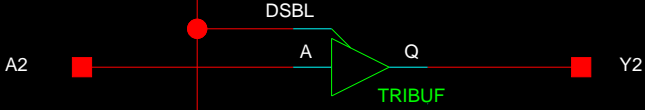
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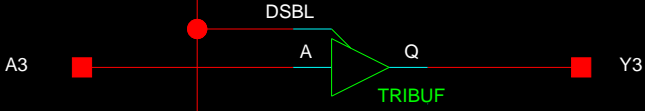
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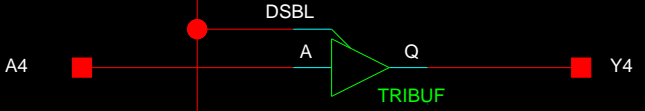
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54HC244

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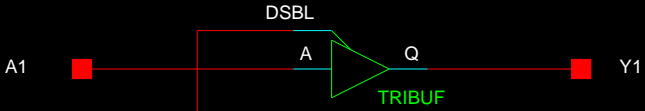
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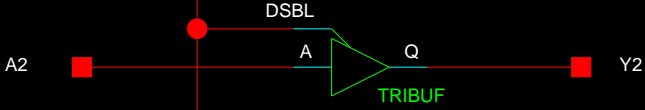
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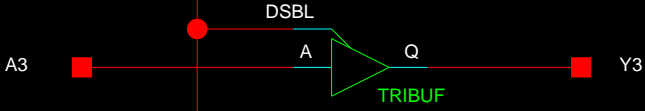
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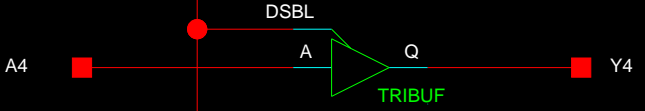
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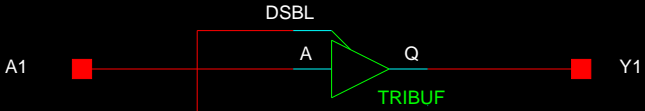
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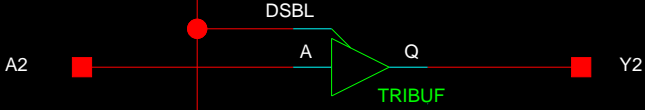
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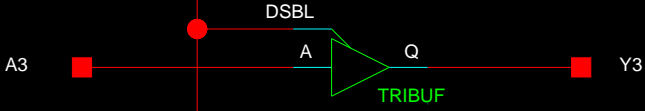
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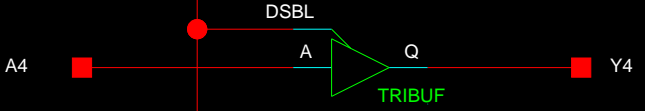
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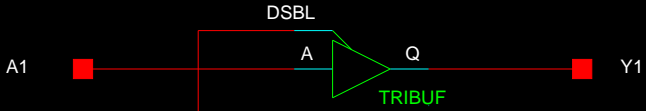
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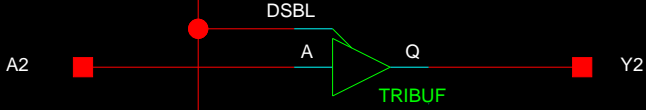
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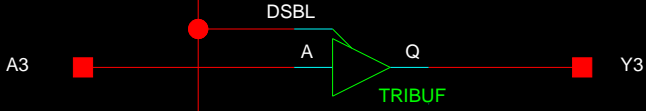
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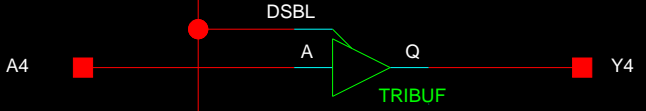
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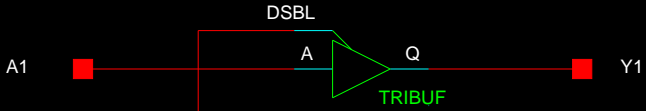
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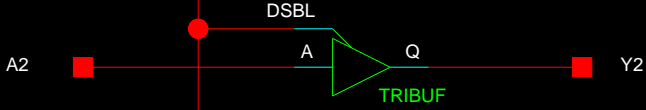
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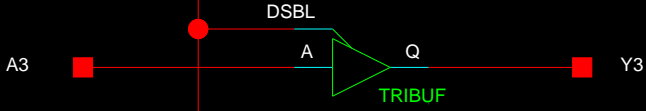
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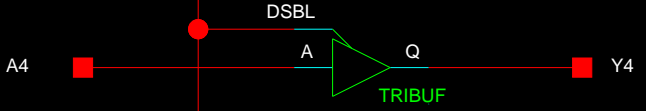
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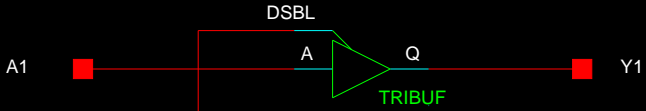
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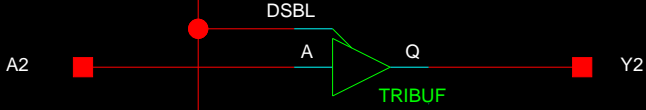
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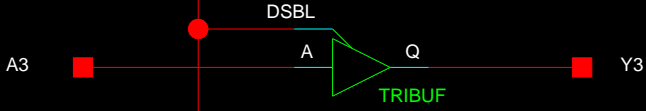
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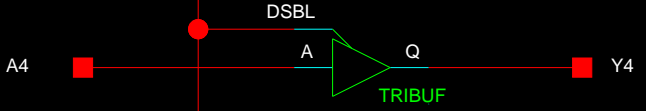
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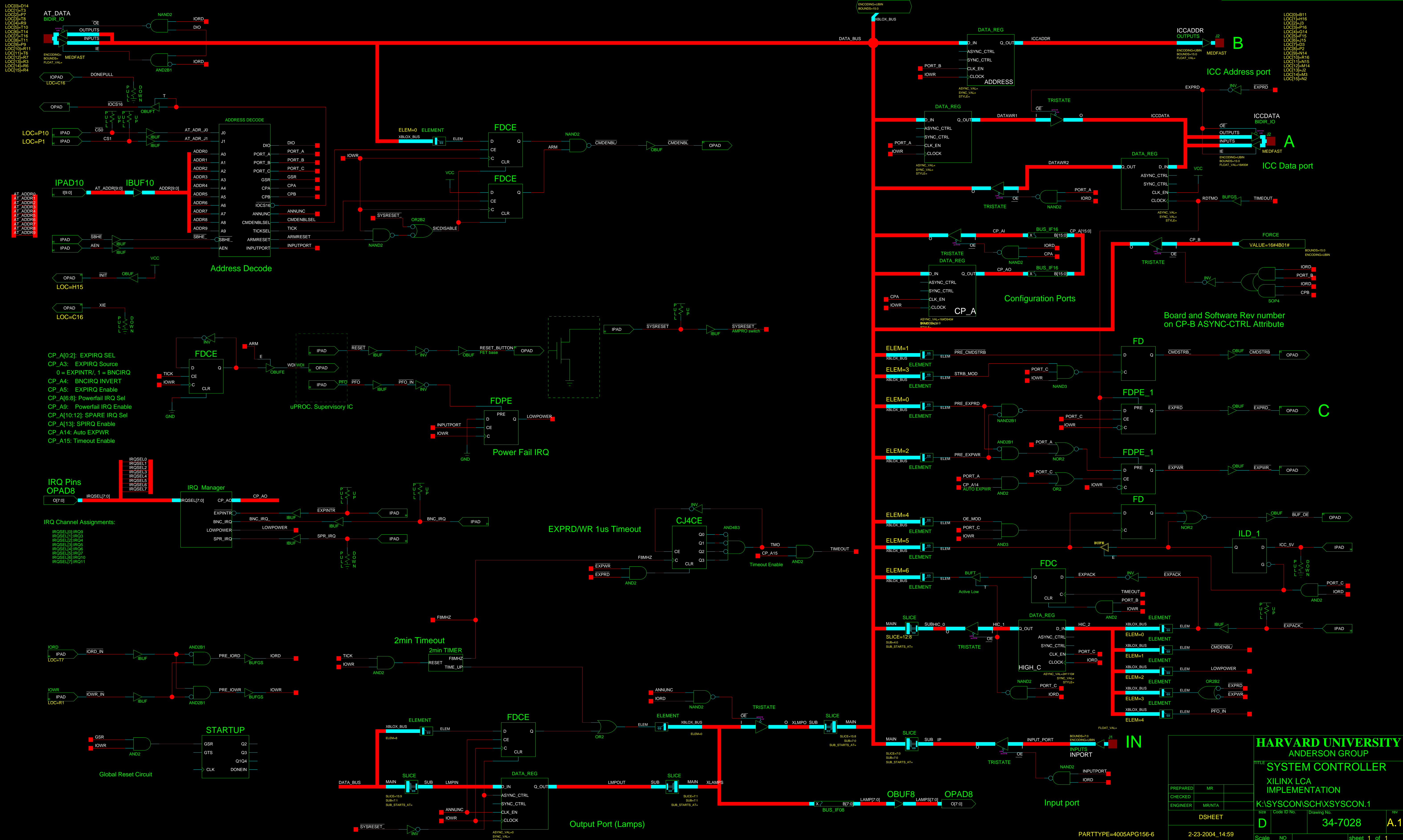
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54HC244

Revisions				
Zone	ltr	Description	Date	Approved
B2		Watchdog Circuit	2/96	NTA
BC4	A.1	Lamp Circuit	2/96	NTA



HARVARD UNIVERSITY
ANDERSON GROUP

TITLE: **SYSTEM CONTROLLER**
XILINX LCA IMPLEMENTATION

PREPARED: MR
CHECKED: MR/NTA
ENGINEER: MR/NTA

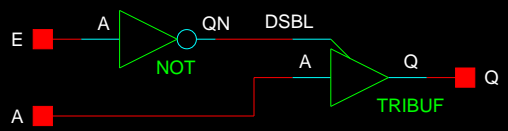
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Scale NO

REV
A.1

sheet 1 of 1

PARTTYPE=4005APG156-6

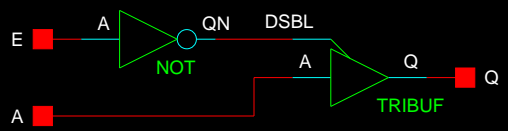


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23Jul92 15:22

SHEET 1 OF 1

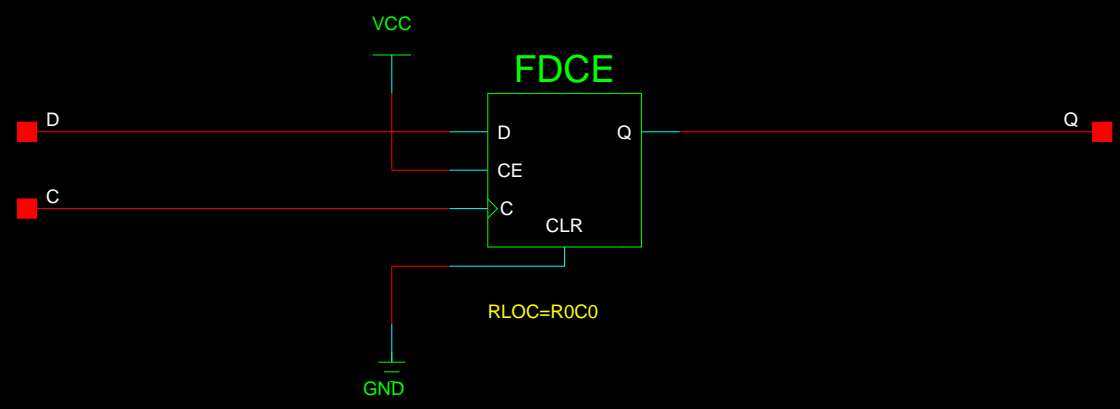


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23Jul92 15:22

SHEET 1 OF 1



Title: XC4000 Family FD Macro

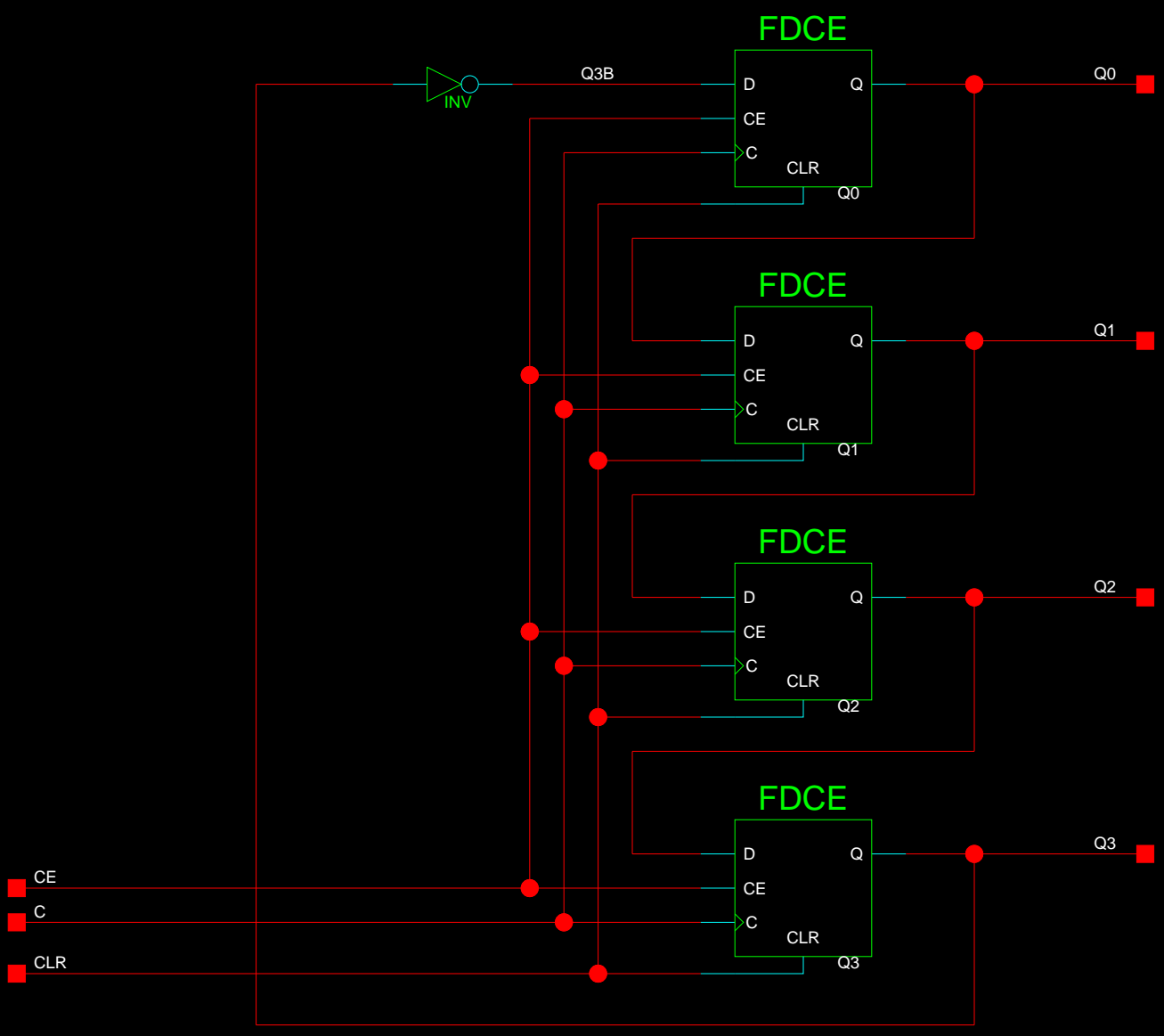
Comments: D Flip-Flop

Date: 23rd December 1992

Ver: 1

Sheet Size: A

Rev: A



Title: XC4000 Family CJ4CE Macro

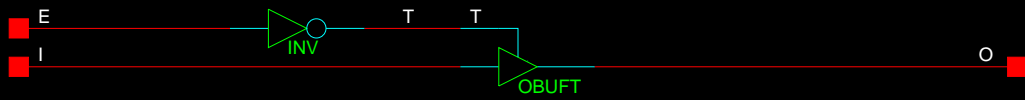
Comments: 4-Bit Johnson Counter with Clock Enable & Async Clear

Date: 25th February 1993

Ver: 1

Sheet Size: A

Rev: A



Title: XC4000 Family OBUFE Macro

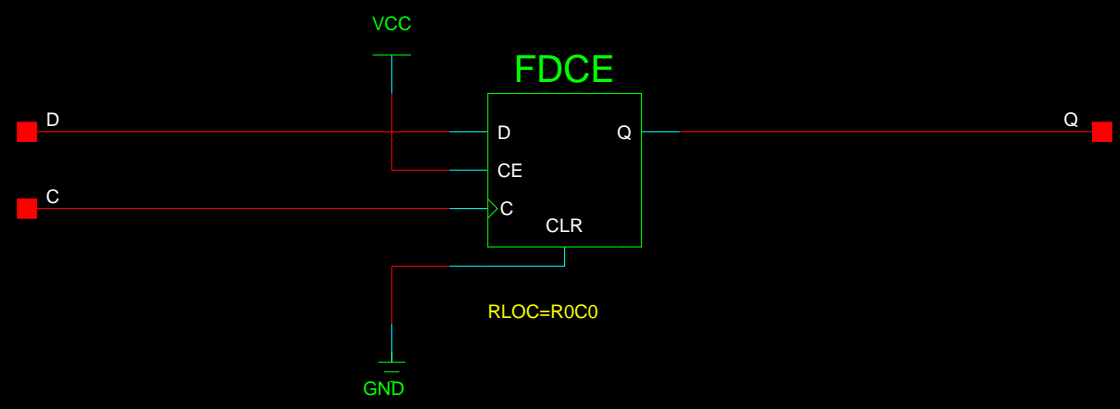
Comments: 3-State Output Buffer with Active High Enable

Date: 22nd February 1993

Ver: 1

Sheet Size: A

Rev: A



Title: XC4000 Family FD Macro

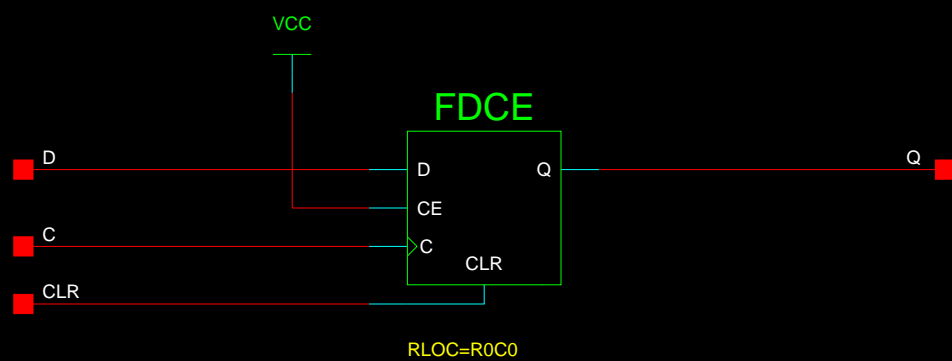
Comments: D Flip-Flop

Date: 23rd December 1992

Ver: 1

Sheet Size: A

Rev: A



Title: XC4000 Family FDC Macro

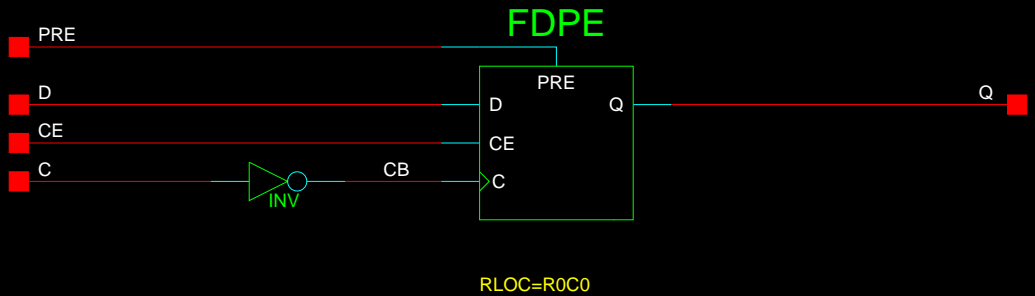
Comments: D Flip-Flop with Asynchronous Clear

Date: 23rd February 1993

Ver: 1

Sheet Size: A

Rev: A



Title: XC4000 Family FDPE_1 Macro

Comments: D Flip-Flop with an inv Clk,
Clk Enable & Asynchronous Preset

Date: 1st March 1993

Ver: 1

Sheet Size: A

Rev: A

D

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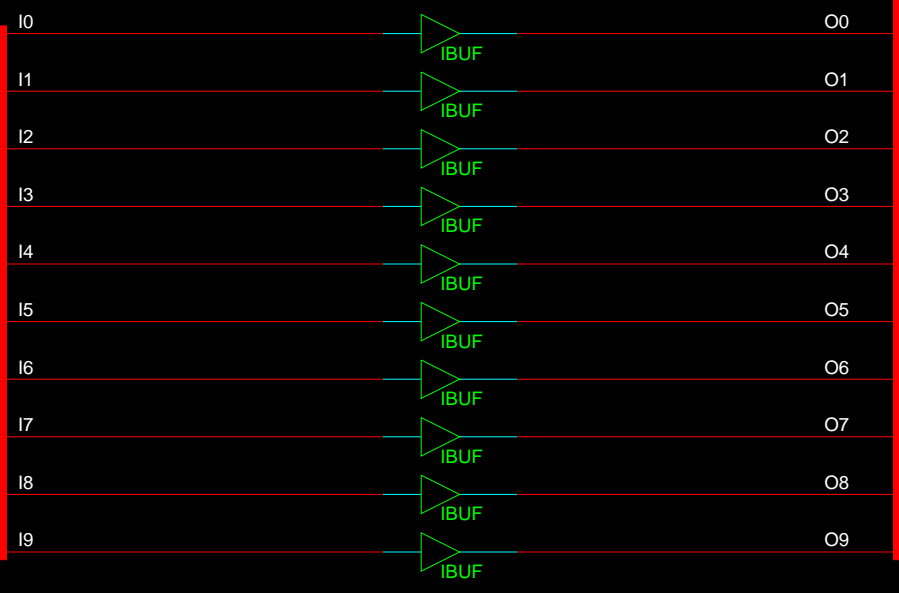
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I[9:0]

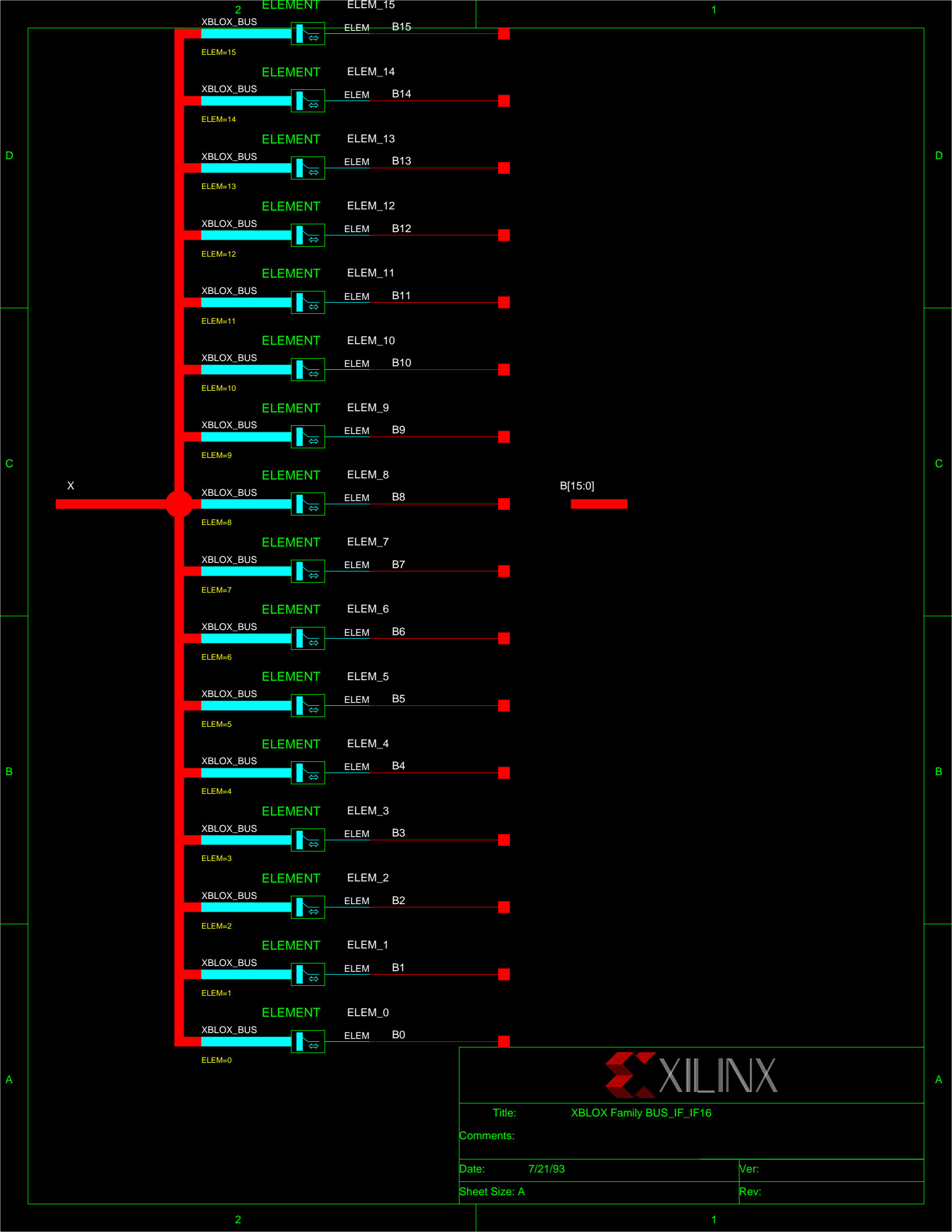


Title: XC4000 Family IBUF8 Macro

Comments: 8-Bit Input Buffer

Date:	25th January 1993	Ver:	1
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Sheet Size: A	Rev:	A
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Title: XBLOX Family BUS_IF_IF16

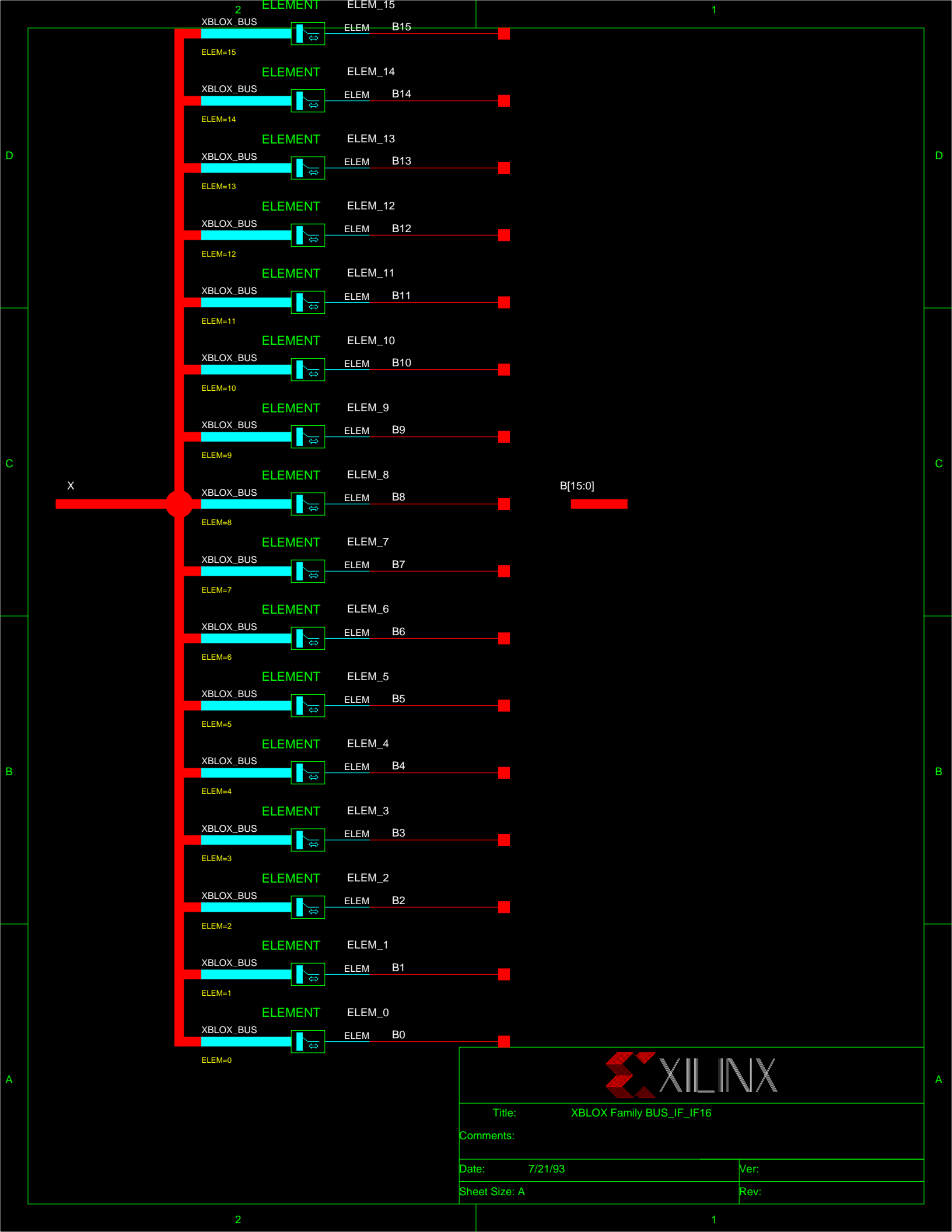
Comments:

Date: 7/21/93

Ver:

Sheet Size: A

Rev:



Title: XBLOX Family BUS_IF_IF16

Comments:

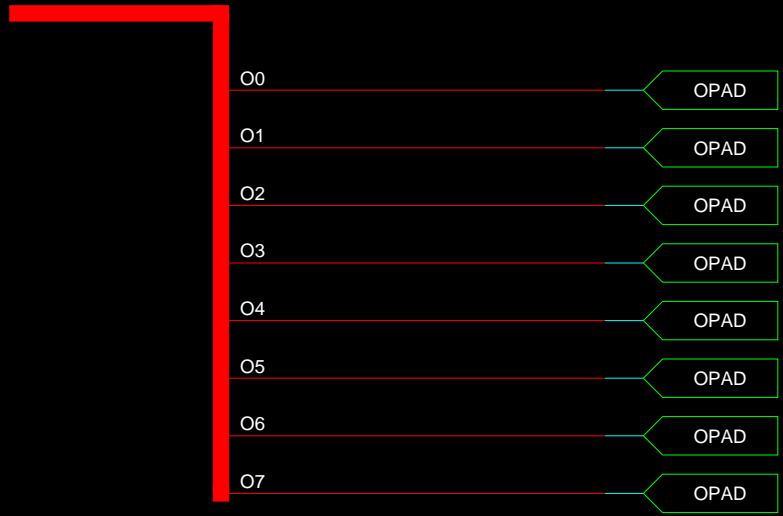
Date: 7/21/93

Ver:

Sheet Size: A

Rev:

O[7:0]



Title: XC4000 Family OPAD8 Macro

Comments: 8-Bit Input Pad

Date: 1st March 1993 Ver: 1

Sheet Size: A Rev: A

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B

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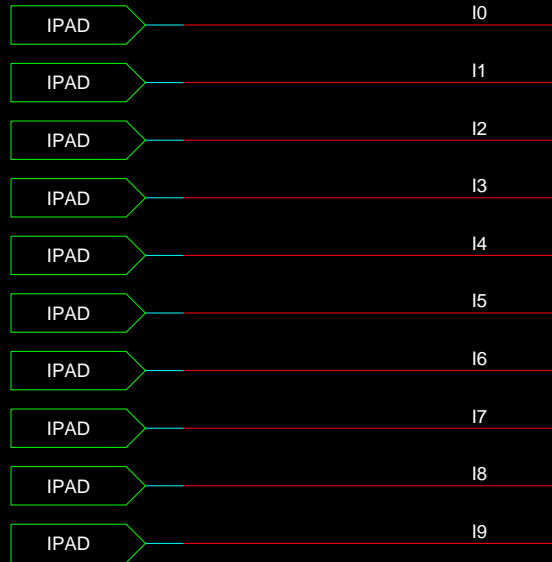
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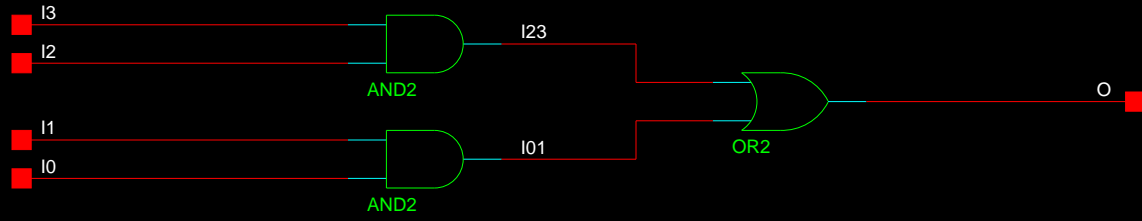


HARVARD UNIVERSITY
ATMOSPHERIC RESEARCH PROJECT

			TITLE			
			XC4000 Family IPAD10 Macro			
			10-bit Input Pad			
PREPARED	MR	26-Jul-94	size	Code ID No.	Drawing No.	rev
CHECKED			A			A
ENGINEER			ASHEET			
4-20-2005_16:20			Scale		sheet	1 of 1

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B



Title: XC4000 Family SOP4 Macro

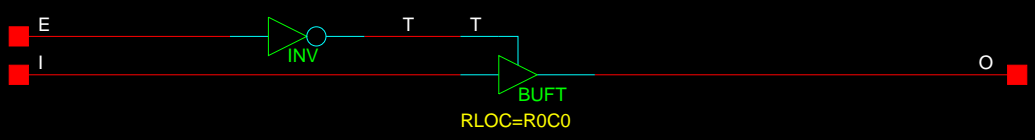
Comments: 4-Input Sum-of-Products

Date: 3rd March 1993

Ver: 1

Sheet Size: A

Rev: A



Title: XC4000 Family BUFE Macro

Comments: 3-State Buffer w/ Active High En

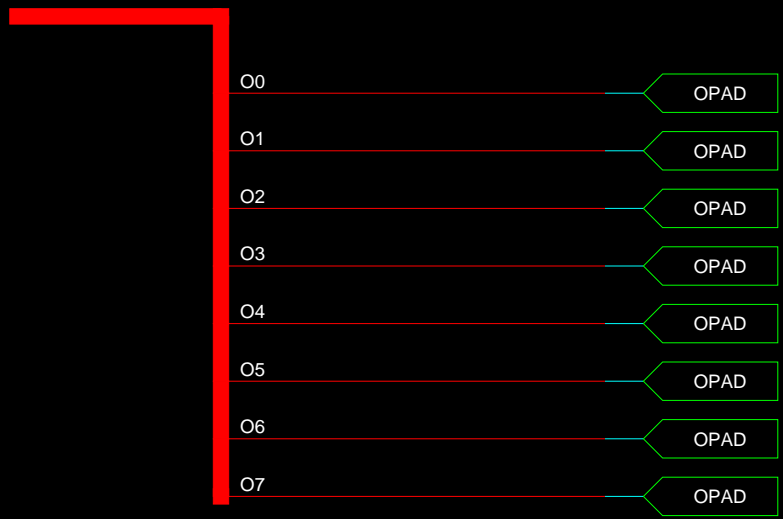
Date: 3rd March 1993

Ver: 1

Sheet Size: A

Rev: A

O[7:0]



Title: XC4000 Family OPAD8 Macro

Comments: 8-Bit Input Pad

Date: 1st March 1993 Ver: 1

Sheet Size: A Rev: A

D

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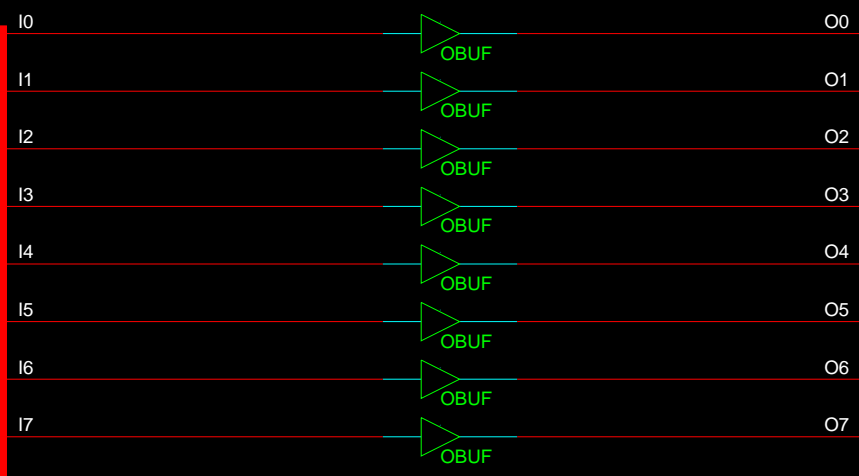
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I[7:0]



Title: XC4000 Family OBUF8 Macro

Comments: 8-Bit Output Buffer

Date:	25th January 1993	Ver:	1
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Sheet Size: A	Rev:	A
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Title: XBLOX Family BUS_IF08

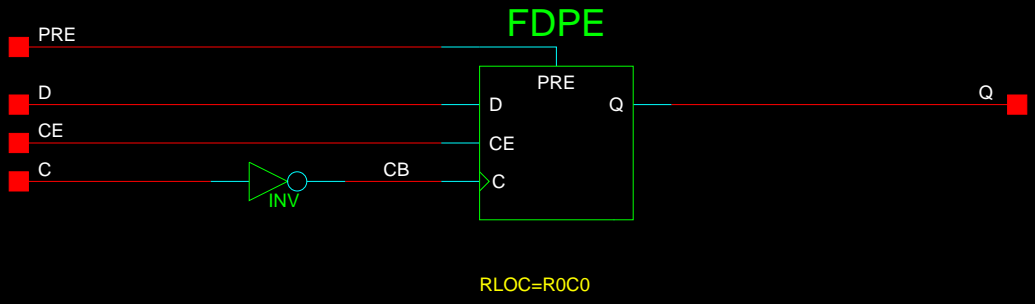
Comments:

Date: 7/21/93

Ver: 1

Sheet Size: A

Rev: A



Title: XC4000 Family FDPE_1 Macro

Comments: D Flip-Flop with an inv Clk,
Clk Enable & Asynchronous Preset

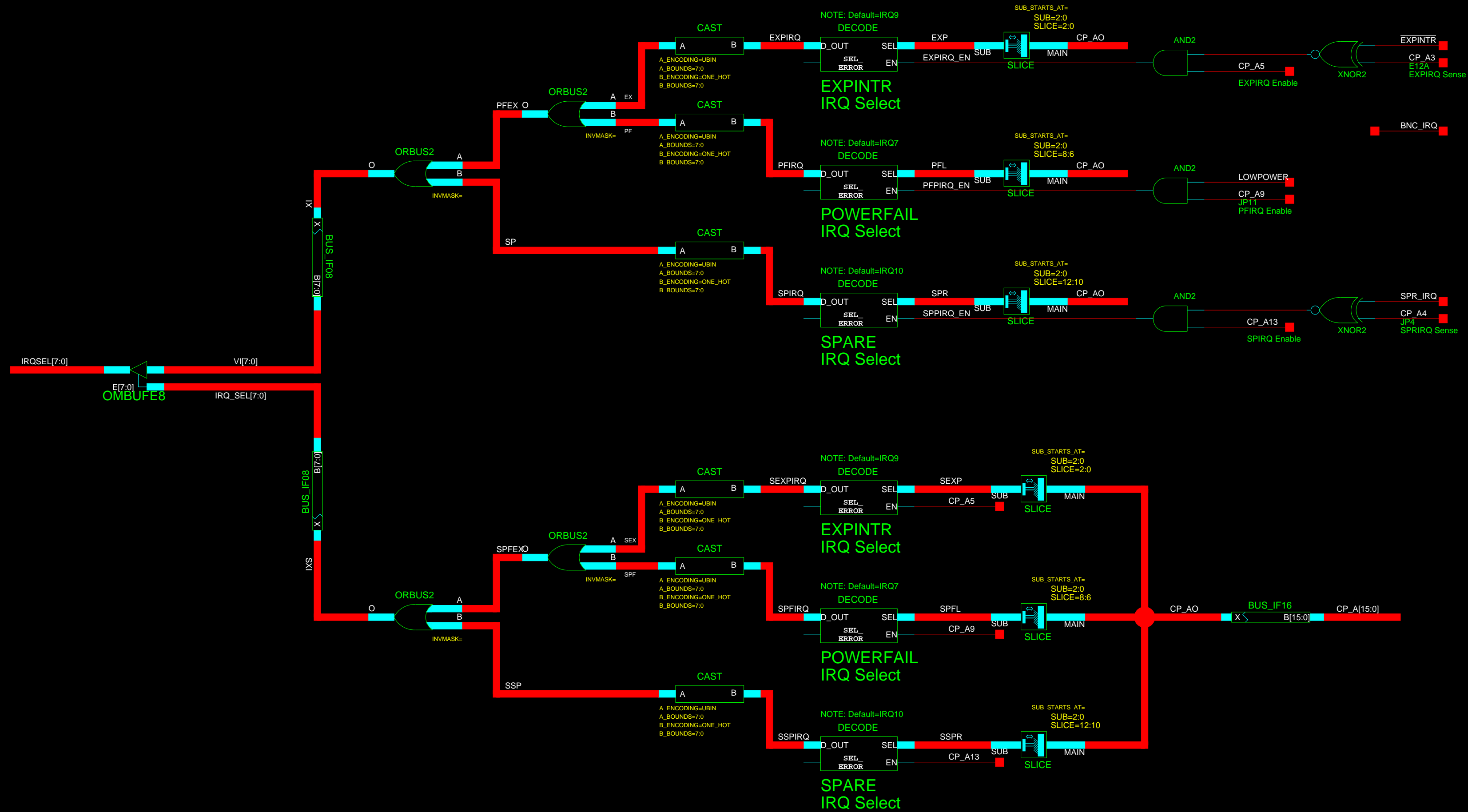
Date: 1st March 1993

Ver: 1

Sheet Size: A

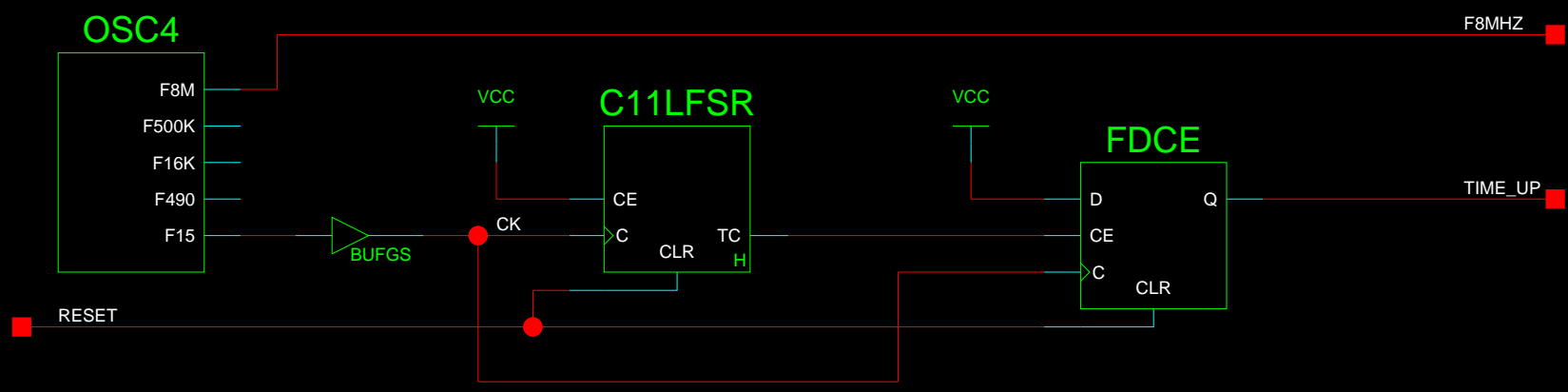
Rev: A

Revisions				
Zone	ltr	Description	Date	Approved



PREPARED		MR	TITLE	HARVARD UNIVERSITY		
		CHECKED			ATMOSPHERIC RESEARCH PROJECT	
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2-21-1997_11:16				C:\SYS\COM\SCH\IRQ_MNGR.1	C:\SYS\COM\SCH\IRQ_MNGR.1	
size	Code ID No.	Drawing No.	rev	34-7028		
Scale		sheet	5 of 7	A		

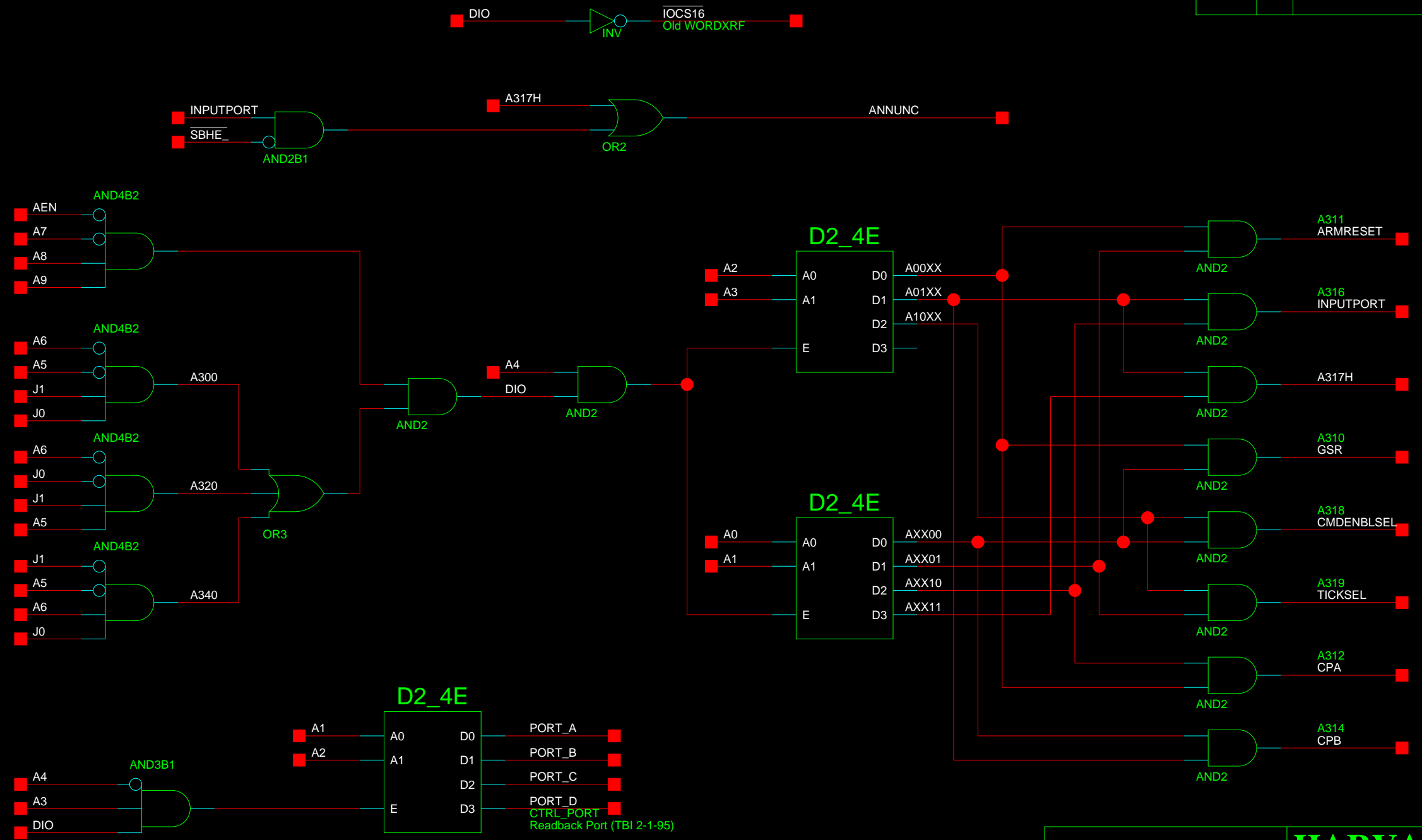
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Zone	Itr	Description	Date	Approved



PREPARED		MR	
CHECKED			
ENGINEER			
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HARVARD UNIVERSITY			
ATMOSPHERIC RESEARCH PROJECT			
TITLE			
2 Minute Timer Subcircuit			
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size	Code ID No.	Drawing No.	rev
B		x23_7028	A
Scale	5-21-1996_13:23		sheet 1 of 1

Revisions				
Zone	Itr	Description	Date	Approved



Port Select

HARVARD UNIVERSITY
 ATMOSPHERIC RESEARCH PROJECT
 TITLE

Address Decoding Logic

PREPARED	MR	APR-95
CHECKED		
ENGINEER	MR	

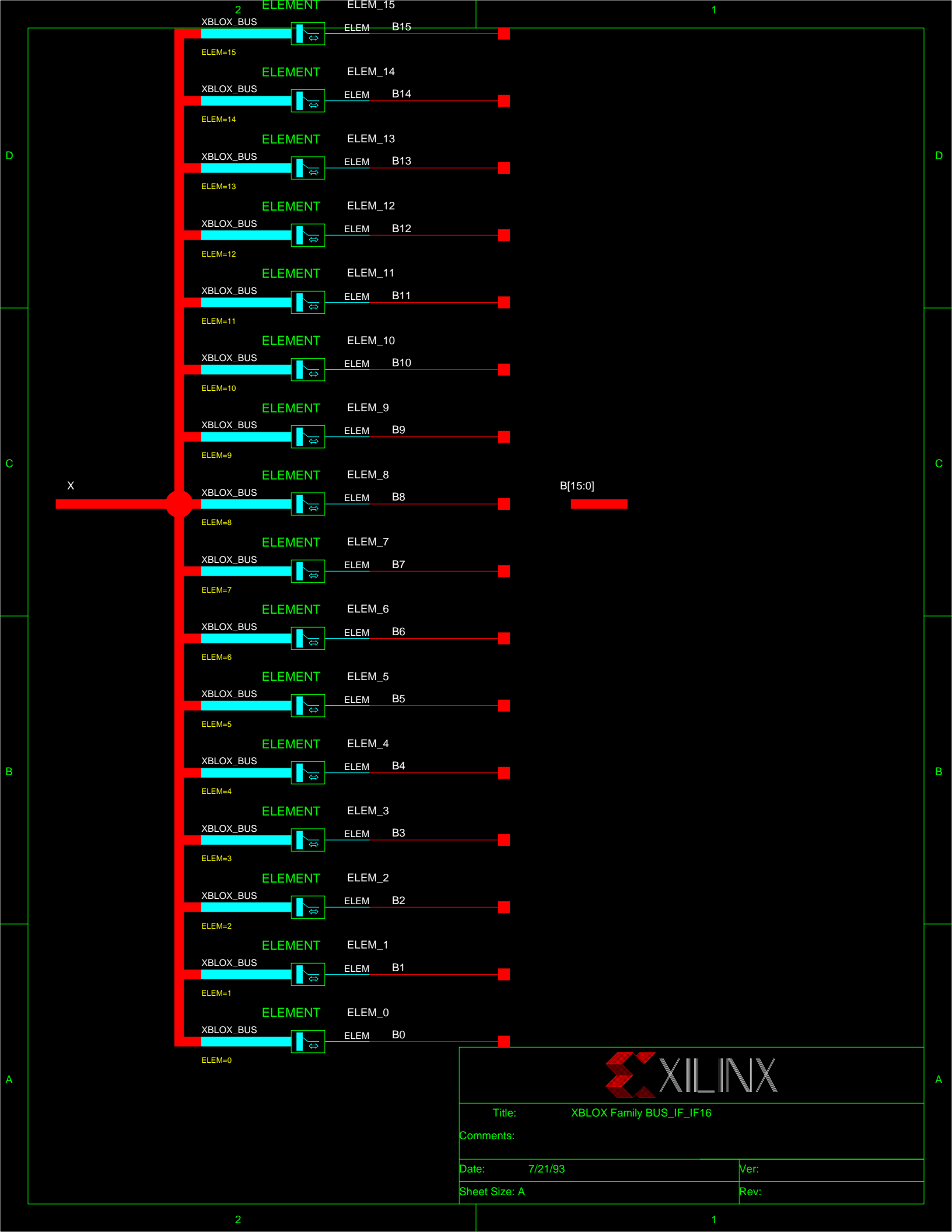
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size	Code ID No.	Drawing No.	rev
B		34-7028	A

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Scale sheet 1 of 1



Title: XBLOX Family BUS_IF_IF16

Comments:

Date: 7/21/93

Ver:

Sheet Size: A

Rev:

A

B

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1

2

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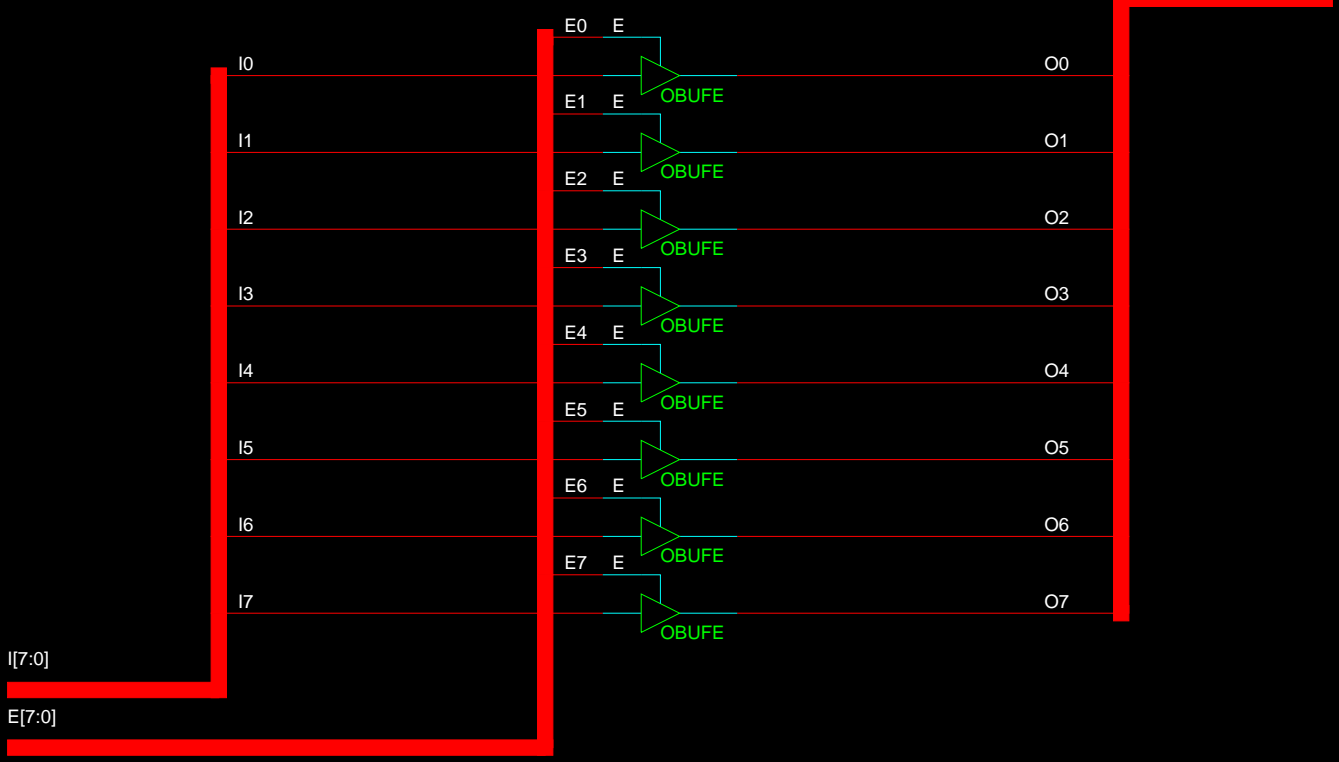
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O[7:0]



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ATMOSPHERIC RESEARCH PROJECT

TITLE
 XC4000 Family OMBUFE8 Macro
 8-Bit 3-State Output Buffer
 w/ Multiple Active High Enable

PREPARED		
CHECKED		
ENGINEER	MR	1-31-95

ASHEET		size	Code ID No.	Drawing No.	rev
		A			A
4-20-2005_16:20		Scale		A	sheet 1 of 1

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B

5

5



Title: XBLOX Family BUS_IF08

Comments:

Date: 7/21/93

Ver: 1

Sheet Size: A

Rev: A



Title: XBLOX Family BUS_IF08

Comments:

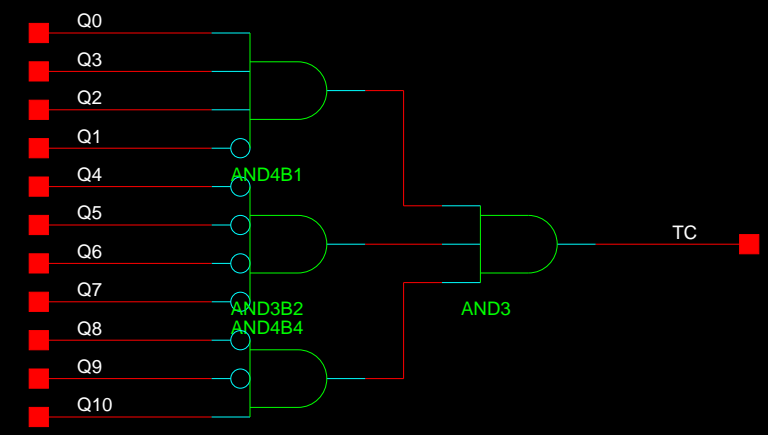
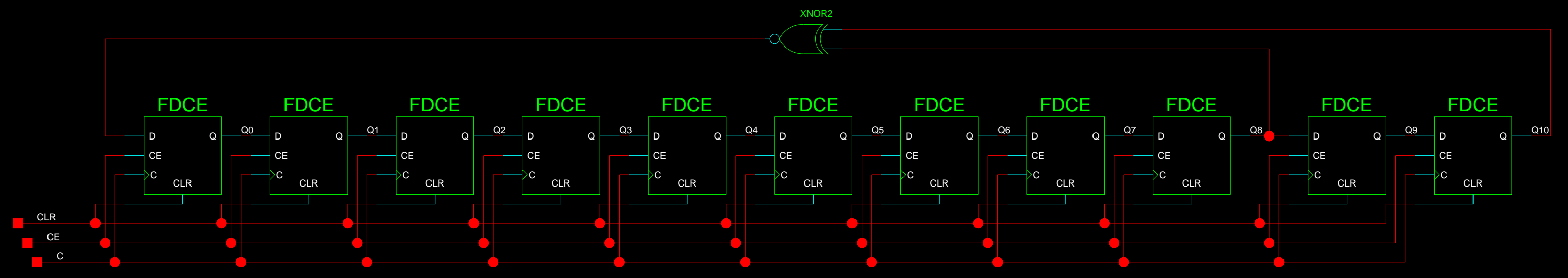
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Ver: 1

Sheet Size: A

Rev: A

Revisions				
Zone	Itr	Description	Date	Approved



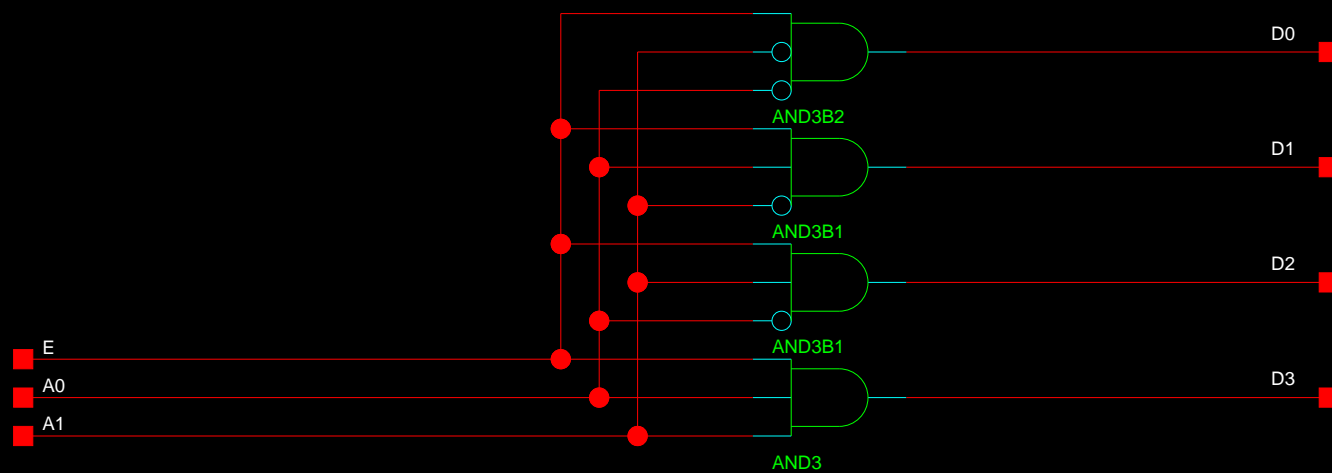
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HARVARD UNIVERSITY
ATMOSPHERIC RESEARCH PROJECT

TITLE

**11-bit Linear Feedback
Shift Register Counter**

size	Code ID No.	Drawing No.	rev
B			A
Scale	sheet 1 of 1		



Title: XC4000 Family D2_4E Macro

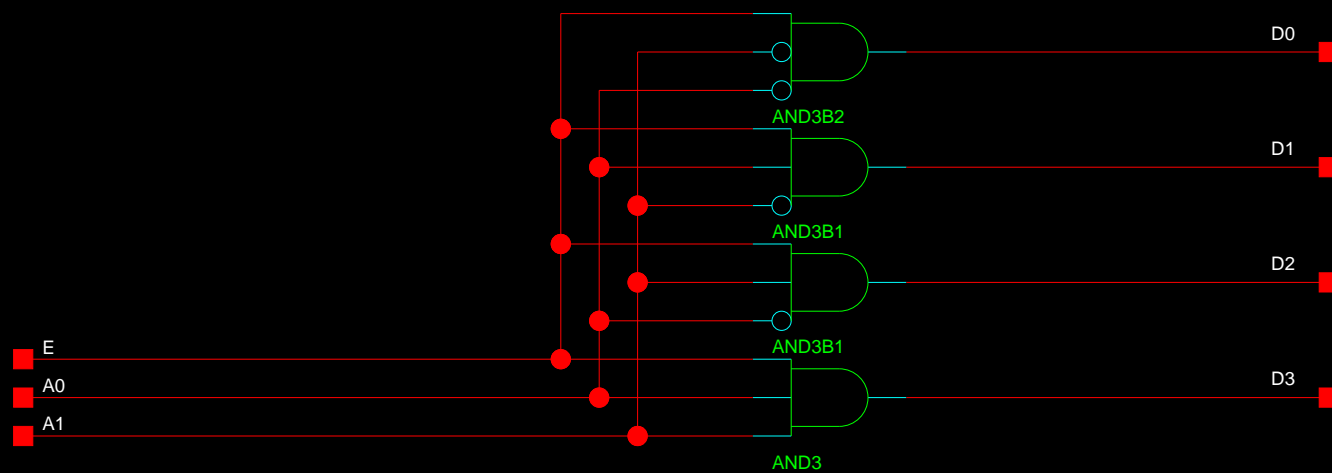
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Demultiplexer w/ Enable

Date: 19th January 1993

Ver: 1

Sheet Size: A

Rev: A



Title: XC4000 Family D2_4E Macro

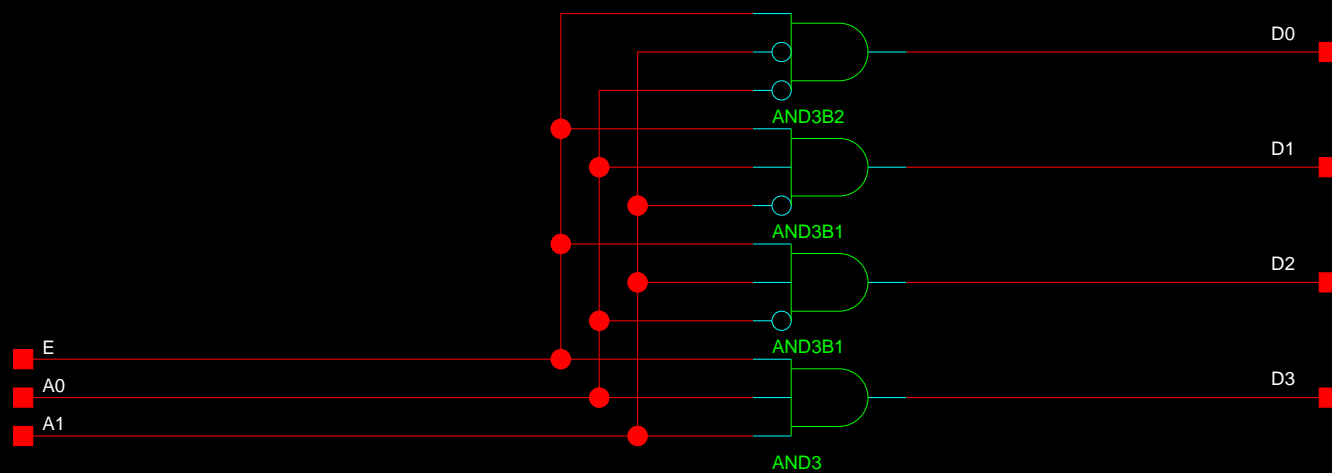
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Date: 19th January 1993

Ver: 1

Sheet Size: A

Rev: A



Title: XC4000 Family D2_4E Macro

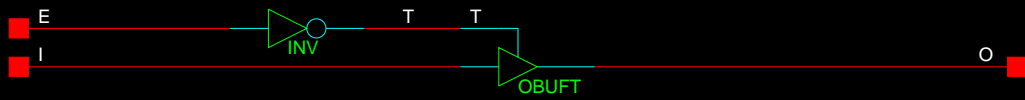
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Date: 19th January 1993

Ver: 1

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Rev: A



Title: XC4000 Family OBUFE Macro

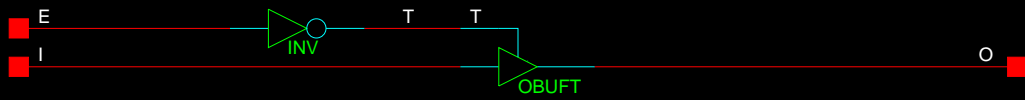
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Date: 22nd February 1993

Ver: 1

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Rev: A



Title: XC4000 Family OBUFE Macro

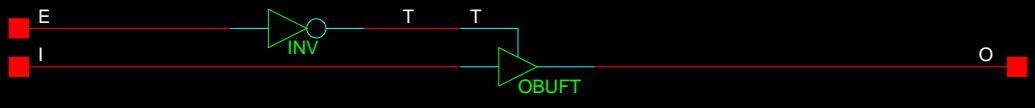
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Ver: 1

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Rev: A



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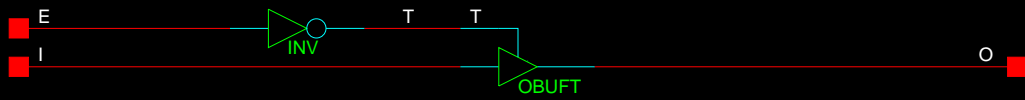
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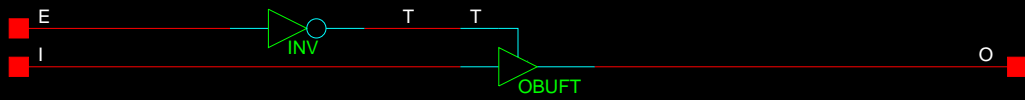
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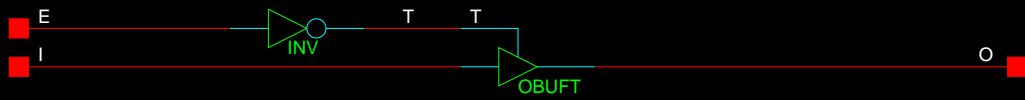
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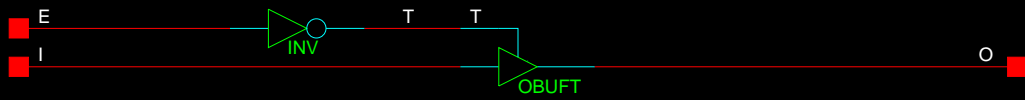
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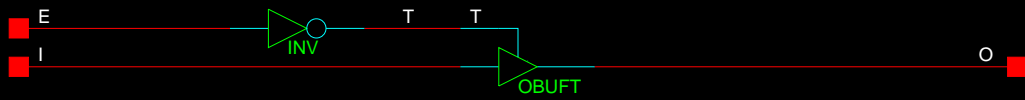
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Rev: A



Title: XC4000 Family OBUFE Macro

Comments: 3-State Output Buffer with Active High Enable

Date: 22nd February 1993

Ver: 1

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Rev: A