BOARD MODIFICATIONS:
Cut Pin 6 off Z1-Z6 pullups, and install 10k pulldown to GND.
BOARD MODIFICATIONS:
Cut Pin 6 off Z1-Z6 pullups, and install 10k pulldown to GND.
BOARD MODIFICATIONS:
Cut Pin 6 off Z1-Z6 pullups, and install 10k pulldown to GND.

HARVARD UNIVERSITY
ATMOSPHERIC RESEARCH PROJECT
IDX_BUF.1
Buffer Block for Indexer

1-19-2006_15:22
BOARD MODIFICATIONS:
Cut Pin 6 off Z1-Z6 pullups, and install 10k pulldown to GND.
BOARD MODIFICATIONS:
Cut Pin 6 off Z1-Z6 pullups, and install 10k pulldown to GND.

HARVARD UNIVERSITY
ATMOSPHERIC RESEARCH PROJECT

IDX_BUF.1
Buffer Block for Indexer

1-19-2006_15:22

IDX_BUF

A
BOARDS MODIFICATIONS:
Cut Pin 6 off Z1-Z6 pullups, and install 10k pulldown to GND.

IDX_BUF.1
Buffer Block for Indexer
XC4000 Family IOPAD16 Macro

Title: 16-bit Input-Output Pad

Comments: 

Date: 23rd February 1993

Sheet Size: A

Rev: A

Copyright (c) 1993, Xilinx Inc.
drawn by KS
XBLOX Family BUS_IF_IF16

Comments:

Date: 7/21/93

Sheet Size: A

Rev:
IBUF
I[15:0]
O[15:0]

IBUF
I0
O0

IBUF
I1
O1

IBUF
I2
O2

IBUF
I3
O3

IBUF
I4
O4

IBUF
I5
O5

IBUF
I6
O6

IBUF
I7
O7

IBUF
I8
O8

IBUF
I9
O9

IBUF
I10
O10

IBUF
I11
O11

IBUF
I12
O12

IBUF
I13
O13

IBUF
I14
O14

IBUF
I15
O15

16-bit Input Buffer
XC4000 Family IPAD16 Macro

16-bit Input Pad

Title:  
Comments:  
Date:  23rd February 1993  
Sheet Size: A  
Rev: A  
Ver:  
Rev:  
Sheet:  
Page: 1
XC4000 Family BUFE Macro

3-State Buffer w/ Active High En

3rd March 1993

Copyright (c) 1993, Xilinx Inc.

drawn by KS

RLOC=R0C0

BUFT

Comments: 3-State Buffer w/ Active High En
HARVARD UNIVERSITY
ATMOSPHERIC RESEARCH PROJECT

IDXCHAN.2
Channel Status, Service Req.

LEGEND:
R: Running
I: INTA
s: Not Requested (NRQD)
s: Serviced

1-19-2006_15:32

A34-7005
Title: XC4000 Family BUFE Macro
Comments: 3-State Buffer w/ Active High En
Date: 3rd March 1993
Sheet Size: A
Rev: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.
XC4000 Family BUFE Macro

3-State Buffer w/ Active High En

3rd March 1993

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Copyright (c) 1993, Xilinx Inc.
XC4000 Family BUFE Macro

3-State Buffer w/ Active High En

RLOC=R0C0

3rd March 1993

Copyright (c) 1993, Xilinx Inc.
XC4000 Family BUFE Macro

3-State Buffer w/ Active High En

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Comment: 3-State Buffer w/ Active High En
XC4000 Family BUFE Macro
3-State Buffer w/ Active High En

RLOC=R0C0

Copyright (c) 1993, Xilinx Inc.
I RDCLK

CLK

RDBK

TRIG

DATA

RIP

DATA

RIP

29th March 1993

LCA Bitstream Readback Controller

drawn by KS

Copyright (c) 1993, Xilinx Inc.
XC4000 Family OBUFE Macro

3-State Output Buffer with Active High Enable

22nd February 1993

drawn by KS
Copyright (c) 1993, Xilinx Inc.
Title: XC4000 Family OBUFE Macro
Comments: 3-State Output Buffer with Active High Enable
Date: 22nd February 1993
Sheet Size: A
Rev: A
Copyright (c) 1993, Xilinx Inc.

drawn by KS

3-State Output Buffer with Active High Enable
A: ARMZERO Input
Z: OZ Qualified Zeroref

00
RESETPOS Output
B "Zero Armed" State
Indexer Channel Step Gen

HARVARD UNIVERSITY
ATMOSPHERIC RESEARCH PROJECT

STEPCLK.1

1-19-2006_15:35

FD_1

FD
XC4000 Family BUFOD Macro

Comments: Open-Drain Buffer

Title: XC4000 Family BUFOD Macro

Date: 6th April 1993

Sheet Size: A

Rev: A

Copyright (c) 1993, Xilinx Inc.

drawn by KS
D Flip-Flop

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A
D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.
Indexer Limit Switches

M2_1B2

OR2

D0

D1

S0

INLIMIT

FD

D

Q

AND2

D

Q

AND2B1

C

F0

OUT

LIMA_NOT

LIMB_NOT

CP0

OUTLIMIT

LIMIT
D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.
XBLOX_FAMILY

TITLE: XBLOX Family BUS_IF05

DATE: 7/21/93

Sheet Size: A

Rev: A
A: ARMZERO Input
Z: OZ Qualified Zeroref

00
- RESETPOS Output
- B "Zero Armed" State
01
10
11

A+Z
AZ

1-19-2006_15:36
Divide by 3/2

Channel Rate Selection

HARVARD UNIVERSITY
ATMOSPHERIC RESEARCH PROJECT
RATEGEN.1

Title: Channel Rate Selection

1-19-2006_15:37

A34-7005
Title: XBLOX Family BUS_IF04

Comments:

Date: 7/21/93
Sheet Size: A
Rev: A
A: ARMZERO Input
Z: OZ Qualified Zeroref

00  

RESETPOS Output
B "Zero Armed" State
D Flip-Flop

XC4000 Family FD Macro

Date: 23rd December 1992
Sheet Size: A

Copyright (c) 1993, Xilinx Inc.
XC4000 Family BUFE4 Macro

4-Bit 3-State Buffer w/ an Active High Enable

23rd February 1993

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Title: XC4000 Family BUFE4 Macro
Comments: 4-Bit 3-State Buffer w/ an Active High Enable
Date: 23rd February 1993
Sheet Size: A

Ver: 1
Rev: A
Title: XC4000 Family BUFE4 Macro
Comments: 4-Bit 3-State Buffer w/ an Active High Enable
Date: 23rd February 1993
Sheet Size: A
XBLOX Family BUS_IF04

Title: XBLOX Family BUS_IF04
Comments:
Date: 7/21/93
Sheet Size: A
Rev: A
A: ARMZERO Input
Z: OZ Qualified Zeroref

00
  |  10
  |  A+Z
  |  01
  |  AZ
  |  11

RESETPOS Output
B "Zero Armed" State

LIMITS.2
Indexer Limit Switches

HARVARD UNIVERSITY
ATMOSPHERIC RESEARCH PROJECT

LIMITS
1-19-2006_15:36
Divide by 3/2

FD

FD

FD_1

M4_1E

M2_1

XOR2

INV

INV

VCC

RC3

RC2

RC1

S0

S1

D0

D1

D2

D3

F0

F1

F2

F3

F4

F[4:0]

RC[3:0]

Rategen.1

Channel Rate Selection
Title: XC4000 Family BUFOD Macro
Comments: Open-Drain Buffer
Date: 6th April 1993
Sheet Size: A
Rev: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.
D Flip-Flop

XC4000 Family FD Macro

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A
Rev: A
FDCE

VCC

D

CE

Q

C

CLR

GND

RLOC=R0C0

D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.
4-Bit 3-State Buffer

XC4000 Family BUFE4 Macro

w/ an Active High Enable

23rd February 1993

drawn by KS

Copyright (c) 1993, Xilinx Inc.
XBLOX Family BUS_IF05

Title: XBLOX Family BUS_IF05
Comments:

Date: 7/21/93
Sheet Size: A
Rev: A
A: ARMZERO Input
Z: OZ Qualified Zeroref
00
RESETPOS Output
B "Zero Armed" State

A34-7005
LIMITS.2
Indexer Limit Switches

HARVARD UNIVERSITY
ATMOSPHERIC RESEARCH PROJECT

1-19-2006_15:36
XC4000 Family BUFOD Macro

Open-Drain Buffer

6th April 1993

drawn by KS
Copyright (c) 1993, Xilinx Inc.
FDCE

D

CE

GND

VCC

RLOC=R0C0

D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Sheet Size: A

Date: 23rd December 1992

Rev: A

Ver: 1

Comments: D Flip-Flop
D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Sheet Size: A

Rev: A

Ver: 1

Date: 23rd December 1992

Comments: D Flip-Flop
4-Bit 3-State Buffer

XC4000 Family BUFE4 Macro

w/ an Active High Enable

23rd February 1993

drawn by KS
Copyright (c) 1993, Xilinx Inc.
HARVARD UNIVERSITY
ATMOSPHERIC RESEARCH PROJECT

IOBITA.1
Data Bus Bit Interface

Prepared: NTA
Checked: NTA
Engineer: NTA

Size: A
Code ID No.: A34-7005
Drawing No.: A
Rev.: A

Date: 1-19-2006
Time: 15:17
Sheet: 7 of 18
IOBITA.1
Data Bus Bit Interface

HARVARD UNIVERSITY
ATMOSPHERIC RESEARCH PROJECT

IOBITA
1-19-2006_15:17
IOBITA.1
Data Bus Bit Interface

HARVARD UNIVERSITY
ATMOSPHERIC RESEARCH PROJECT

PREPARED
CHECKED
ENGINEER

IOBITA
A
1-19-2006_15:17

Code ID No. A34-7005
Drawing No. A
REV A

Sheet 1 of 5
FDCE

D CE Q

VCC

GND

RLOC=R0C0

XC4000 Family FD Macro

D Flip-Flop

23rd December 1992

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Title: XC4000 Family FD Macro
Comments: D Flip-Flop

Date: 23rd December 1992
Sheet Size: A

Ver: 1
Rev: A
FDCE

D

C

CLR

Q

GND

VCC

RLOC=R0C0

D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.
drawn by KS

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A
Ver: 1
Rev: A
LEGEND:

S: Step Clock Input
W: Write Input
L: Latch Output
K: Counter Clock Output
LD: Latched State
KD: Clocked State

10x0

x in a state block indicates
"either" as a destination and
"both" as a source.
XC4000 Family BUFE16 Macro

w/ an Active High Enable

16-Bit 3-State Buffer

23rd February 1993

Copyright (c) 1993, Xilinx Inc.

drawn by KS
Copyright (c) 1993, Xilinx Inc.

Title: XC4000 Family BUFE16 Macro
Comments: w/ an Active High Enable
Date: 23rd February 1993
Rev: 1
Sheet Size: A
XC4000 Family INV16 Macro
16-bit Inverter

Title: XC4000 Family INV16 Macro
Comments: 16-bit Inverter

Date: 22nd February 1993
Ref: 1
Sheet Size: A
Rev: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.
Counter w/ Clk En & Async Clr (using CY4)

16-Bit Cascadable, Loadable Binary

XC4000 Family CC16CLE Macro
D Flip-Flop w/ an inverted Clock

Title: XC4000 Family FD_1 Macro
Comments: D Flip-Flop w/ an inverted Clock
Date: 1st March 1993
Sheet Size: A
Rev: A
FDCE

D
CE
Q

D Flip-Flop

XC4000 Family FD Macro

23rd December 1992
LEGEND:

S: Step Clock Input
W: Write Input
L: Latch Output
K: Counter Clock Output
LD: Latched State
KD: Clocked State

x in a state block indicates "either" as a destination and "both" as a source.

State Machine for Counter Latch
XC4000 Family BUFE16 Macro

16-Bit 3-State Buffer

w/ an Active High Enable

Title: XC4000 Family BUFE16 Macro
Comments: 16-Bit 3-State Buffer w/ an Active High Enable
Date: 23rd February 1993
Sheet Size: A
Rev: 1

Copyright (c) 1993, Xilinx Inc.

drawn by KS
Copyright (c) 1993, Xilinx Inc.
XC4000 Family INV16 Macro

Title: 16-bit Inverter

Comments: drawn by KS

Date: 22nd February 1993

Sheet Size: A

Copyright (c) 1993, Xilinx Inc.
D Flip-Flop w/ an inverted Clock

XC4000 Family FD_1 Macro

D, Ce, Gnd, Vcc, Rloc=R0C0

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Title: XC4000 Family FD_1 Macro
Comments: D Flip-Flop w/ an inverted Clock
Date: 1st March 1993
Sheet Size: A
Rev: A
Ver: 1
D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Sheet Size: A

Rev: A

Comments: D Flip-Flop

Date: 23rd December 1992

Ver: 1
D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992
Sheet Size: A

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Copyright (c) 1993, Xilinx Inc.
Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A
Rev: A

Copyright (c) 1993, Xilinx Inc.
drawn by KS.
D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.

RLOC=R0C0

VCC

GND

FDCE

D

CE

C

CLR

Q
XC4000 Family M2_1B2 Macro

D0 & D1 Inverted

2-to-1 Multiplexer w/ D0 & D1 Inverted

1st March 1993
FDCE

D
CE
C
CLR

VCC
GND
RLOC=R0C0

D
Q
Q
FDCE

D -> Q

CE -> D

C

CLR

VCC

GND

RLOC=R0C0

Copyright (c) 1993, Xilinx Inc.
drawn by KS

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A
Rev: A
Ver: 1
D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Title:      XC4000 Family FD Macro
Comments:   D Flip-Flop
Date:      23rd December 1992
Sheet Size: A

Rev:  A
Ver:  1
LEGEND:

S: Step Clock Input
W: Write Input
L: Latch Output
K: Counter Clock Output
LD: Latched State
KD: Clocked State

x in a state block indicates "either" as a destination and "both" as a source.

State Machine for Counter Latch
XC4000 Family BUFE16 Macro

16-Bit 3-State Buffer w/ an Active High Enable

Title: XC4000 Family BUFE16 Macro
Comments: 16-Bit 3-State Buffer w/ an Active High Enable
Date: 23rd February 1993
Sheet Size: A

Copyright (c) 1993, Xilinx Inc.
drawn by KS
Copyright (c) 1993, Xilinx Inc.
D Flip-Flop w/ an inverted Clock

XC4000 Family FD_1 Macro

Date: 1st March 1993

Comments: D Flip-Flop w/ an inverted Clock
D Flip-Flop w/ an inverted Clock

Title: XC4000 Family FD_1 Macro
Comments: D Flip-Flop w/ an inverted Clock

Date: 1st March 1993
Sheet Size: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.
FDCE

D

CE

Q

C

CLR

VCC

GND

RLOC=R0C0

D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A
D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Sheet Size: A

Rev: 1
Ver: 1

Date: 23rd December 1992
Sheet Size: A
D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.
drawn by KS

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A

Ver: 1
Rev: A
FDCE

D
CE
Q
Q

D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.
drawn by KS

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A

Ver: 1
Rev: A
FDCE

D
CE
Q
CLR

VCC
GND
RLOC=R0C0

D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.
drawn by KS

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A
LEGEND:
- S: Step Clock Input
- W: Write Input
- L: Latch Output
- K: Counter Clock Output
- LD: Latched State
- KD: Clocked State

x in a state block indicates
"either" as a destination and
"both" as a source.

State Machine for Counter Latch
Counter w/ Clk En & Async Clr (using CY4)

Title: 14th June 1993

RLOC=R6C1.G
RLOC=R8C1.FFX
RLOC=R8C1.FFY
RLOC=R7C1.FFX
RLOC=R6C1.FFY
RLOC=R4C1.FFX
RLOC=R3C1.FFY
RLOC=R2C1.F

Sheet Size: E

Counter w/ Clk En & Async Clr (using CY4)
XC4000 Family BUFE16 Macro

w/ an Active High Enable

16-Bit 3-State Buffer

Title: XC4000 Family BUFE16 Macro
Comments: w/ an Active High Enable

Date: 23rd February 1993
Rev: 1

Sheet Size: A

Copyright (c) 1993, Xilinx Inc.
drawn by KS

Rev: A
D Flip-Flop w/ an inverted Clock

XC4000 Family FD_1 Macro

Date: 1st March 1993

Comments: D Flip-Flop w/ an inverted Clock

drawn by KS
Copyright (c) 1993, Xilinx Inc.
D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Sheet Size: A

Rev: A

Ver: 1

Date: 23rd December 1992

Comments: D Flip-Flop
D Flip-Flop w/ an inverted Clock

FDCE

D  Q
CE  Q
G  CLR
VCC
GND

RLOC=R0C0

inv

drawn by KS
Copyright (c) 1993, Xilinx Inc.
D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A

RLOC=R0C0
GND

D

Q

CE

CLR

VCC
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
4-to-1 Multiplexer with Enable

Title: XC4000 Family M4_1E Macro
Comments: 4-to-1 Multiplexer with Enable

Date: 1st December 1994  Ver: 1
Sheet Size: A  Rev: B

Copyright (c) 1993, Xilinx Inc.

drawn by KS
Copyright (c) 1993, Xilinx Inc.
XC4000 Family M2_1 Macro
2-to-1 Multiplexer

D0
S0
D1
M0
M1
OR2
AND2
AND2B1

drawn by KS
Copyright (c) 1993, Xilinx Inc.
14th December 1992

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A
Ver: 1
FDCE

D  Q  CE  Q

D  C  CLR

VCC

GND

RLOC=R0C0

Xilinx

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A

Copyright (c) 1993, Xilinx Inc.
Title: XC4000 Family M2_1B2 Macro
Comments: 2-to-1 Multiplexer w/ D0 & D1 Inverted
Date: 1st March 1993
Sheet Size: A
Rev: A

D0 -> AND2B2 (M0) -> OR2 -> O
S0 -> AND2B2 (M0)
D1 -> AND2B1 (M1) -> OR2
D0
S0
D1

 AND2B2

 M0

 OR2

 AND2B1

 M1

 O

Title: XC4000 Family M2_1B2 Macro
Comments: 2-to-1 Multiplexer w/ D0 & D1 Inverted
Date: 1st March 1993
Sheet Size: A
FDCE

D
CE
Q
C
CLR

VCC
GND
RLOC=R0C0

D Flip-Flop

XC4000 Family FD Macro

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A
Rev: A

Copyright (c) 1993, Xilinx Inc.
LEGEND:

S: Step Clock Input
W: Write Input
L: Latch Output
K: Counter Clock Output
LD: Latched State
KD: Clocked State

x in a state block indicates
"either" as a destination and
"both" as a source.

State Machine for Counter Latch
XC4000 Family BUFE16 Macro
w/ an Active High Enable

16-Bit 3-State Buffer

Title:
Comments:

Date: 23rd February 1993
Rev: 1

Sheet Size: A

Copyright (c) 1993, Xilinx Inc.
drawn by KS

E
D Flip-Flop w/ an inverted Clock

Title: XC4000 Family FD_1 Macro
Comments: D Flip-Flop w/ an inverted Clock
Date: 1st March 1993
Sheet Size: A
Rev: A

Copyright (c) 1993, Xilinx Inc.
D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.
drawn by KS
Copyright (c) 1993, Xilinx Inc.

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A
Rev: A
D Flip-Flop w/ an inverted Clock

Title: XC4000 Family FD_1 Macro
Comments: D Flip-Flop w/ an inverted Clock

Date: 1st March 1993
Sheet Size: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.
XC4000 Family M2_1 Macro

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Version: 1
Revision: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer
Comments: drawn by KS
Copyright (c) 1993, Xilinx Inc.

Date: 14th December 1992
Sheet Size: A
Rev: 1
Ver: A
D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.
drawn by KS
Sheet Size: A

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A
Rev: A

RLOC=R0C0
XC4000 Family M2_1B2 Macro

2-to-1 Multiplexer w/ D0 & D1 Inverted

Date: 1st March 1993

Sheet Size: A
Rev: A
XC4000 Family M2_1B2 Macro

2-to-1 Multiplexer w/ D0 & D1 Inverted

D0

S0

D1

O

AND2B2

AND2B1

M0

M1

OR2

Title: XC4000 Family M2_1B2 Macro
Comments: 2-to-1 Multiplexer w/ D0 & D1 Inverted
Date: 1st March 1993
Sheet Size: A
FDCE

D → Q
CE
C
CLR

VCC
GND

RLOC=R0C0

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A

Rev: 1
D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.
Legend:

- **S**: Step Clock Input
- **W**: Write Input
- **L**: Latch Output
- **K**: Counter Clock Output
- **LD**: Latched State
- **KD**: Clocked State

10x0

x in a state block indicates "either" as a destination and "both" as a source.

State Machine for Counter Latch
XC4000 Family BUFE16 Macro

with an Active High Enable

16-Bit 3-State Buffer

Title:

Comments:

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Date: 23rd February 1993

Sheet Size: A

Rev: A
D Flip-Flop w/ an inverted Clock

XC4000 Family FD_1 Macro

D Flip-Flop w/ an inverted Clock

drawn by KS
Copyright (c) 1993, Xilinx Inc.

Title: XC4000 Family FD_1 Macro
Comments: D Flip-Flop w/ an inverted Clock
Date: 1st March 1993
Sheet Size: A
Rev: A
D Flip-Flop
XC4000 Family FD Macro

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A

Copyright (c) 1993, Xilinx Inc.
drawn by KS

Sheet Size: A
Rev: 1
FDCE

D

CE

Q

C

CLR

VCC

GND

RLOC=R0C0
D Flip-Flop
XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.
drawn by KS

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A
Rev: 1
Title: XC4000 Family BUFE Macro
Comments: 3-State Buffer w/ Active High En
Date: 3rd March 1993
Sheet Size: A
Rev: A
Copyright (c) 1993, Xilinx Inc.

XC4000 Family BUFE Macro
3-State Buffer w/ Active High En

Title: XC4000 Family BUFE Macro
Comments: 3-State Buffer w/ Active High En
Date: 3rd March 1993
Sheet Size: A
Rev: A
Copyright (c) 1993, Xilinx Inc.
XC4000 Family OBUFE Macro

3-State Output Buffer with Active High Enable

Date: 22nd February 1993

Sheet Size: A

Rev: A

Copyright (c) 1993, Xilinx Inc.

drawn by KS
XC4000 Family BUFE Macro

3-State Buffer w/ Active High En

3rd March 1993

Copyright (c) 1993, Xilinx Inc.

drawn by KS

 XC4000 Family BUFE Macro
 Comments: 3-State Buffer w/ Active High En
 Date: 3rd March 1993  Ver: 1
 Sheet Size: A  Rev: A

RLOC=R0C0
XC4000 Family OBUFE Macro

3-State Output Buffer with Active High Enable

22nd February 1993

drawn by KS
Copyright (c) 1993, Xilinx Inc.
XC4000 Family BUFE Macro

3-State Buffer w/ Active High En

3rd March 1993

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Title: XC4000 Family BUFE Macro
Comments: 3-State Buffer w/ Active High En
Date: 3rd March 1993
Sheet Size: A
Ver: 1
Rev: A
XC4000 Family OBUFE Macro

3-State Output Buffer with Active High Enable

22nd February 1993

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Title: XC4000 Family OBUFE Macro
Comments: 3-State Output Buffer with Active High Enable
Date: 22nd February 1993
Sheet Size: A

Ver: 1
Rev: A
XC4000 Family OBUFE Macro

Title: 3-State Output Buffer with Active High Enable

Comments:

Date: 22nd February 1993
Sheet Size: A

Copyright (c) 1993, Xilinx Inc.

drawn by KS

drawn by KS, Xilinx Inc.
XC4000 Family BUFE Macro

3-State Buffer w/ Active High En

RLOC=R0C0

3rd March 1993

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Copyright (c) 1993, Xilinx Inc.
Title: XC4000 Family OBUFE Macro
Comments: 3-State Output Buffer with Active High Enable
Date: 22nd February 1993
Sheet Size: A
Rev: A

Copyright (c) 1993, Xilinx Inc.

drawn by KS

XC4000 Family OBUFE Macro
3-State Output Buffer with Active High Enable

Date: 22nd February 1993
Sheet Size: A
Rev: A

Copyright (c) 1993, Xilinx Inc.
XC4000 Family BUFE Macro

3-State Buffer w/ Active High En

3rd March 1993
XC4000 Family OBUFE Macro

3-State Output Buffer with
Active High Enable

Date: 22nd February 1993
Sheet Size: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.
XC4000 Family OBUFE Macro
3-State Output Buffer with Active High Enable

drawn by KS
Copyright (c) 1993, Xilinx Inc.
XC4000 Family BUFE Macro

Title: XC4000 Family BUFE Macro
Comments: 3-State Buffer w/ Active High En
Date: 3rd March 1993
Sheet Size: A
Copyright (c) 1993, Xilinx Inc.

drawn by KS
Copyright (c) 1993, Xilinx Inc.
3-State Output Buffer with Active High Enable

Title: XC4000 Family OBUFE Macro
Comments: 3-State Output Buffer with Active High Enable
Date: 22nd February 1993
Sheet Size: A
Copyright (c) 1993, Xilinx Inc.
XC4000 Family BUFE Macro
3-State Buffer w/ Active High En

RLOC=R0C0

3rd March 1993
XC4000 Family OBUFE Macro

3-State Output Buffer with Active High Enable

Date: 22nd February 1993

Copyright (c) 1993, Xilinx Inc.
XC4000 Family BUFE Macro
3-State Buffer w/ Active High En

Date: 3rd March 1993
Sheet Size: A
Rev: A
XC4000 Family BUFE Macro

3-State Buffer w/ Active High En

Date: 3rd March 1993

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Comments: 3-State Buffer w/ Active High En

Sheet Size: A

Rev: A

Ver: 1
XC4000 Family OBUFE Macro

3-State Output Buffer with Active High Enable

Date: 22nd February 1993
Ver: 1
Sheet Size: A
Rev: A
Title: XC4000 Family OBUFTE Macro
Comments: 3-State Output Buffer with Active High Enable
Date: 22nd February 1993
Sheet Size: A
Rev: A

Copyright (c) 1993, Xilinx Inc.

drawn by KS

XC4000 Family OBUFTE Macro
3-State Output Buffer with Active High Enable
22nd February 1993
Sheet Size: A
Rev: A

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Title: XC4000 Family OBUFTE Macro
Comments: 3-State Output Buffer with Active High Enable
Date: 22nd February 1993
Sheet Size: A
Rev: A

Copyright (c) 1993, Xilinx Inc.

drawn by KS
XC4000 Family BUFE Macro

Comments: 3-State Buffer w/ Active High En

Date: 3rd March 1993
Sheet Size: A
Rev: A

Title: XC4000 Family BUFE Macro
Comments: 3-State Buffer w/ Active High En
Date: 3rd March 1993
Sheet Size: A
Rev: A
XC4000 Family OBUFE Macro

3-State Output Buffer with Active High Enable

Date: 22nd February 1993
Sheet Size: A

Title: XC4000 Family OBUFE Macro
Comments: 3-State Output Buffer with Active High Enable

drawn by KS
Copyright (c) 1993, Xilinx Inc.
XC4000 Family BUFE Macro

3-State Buffer w/ Active High En

3rd March 1993

Copyright (c) 1993, Xilinx Inc.
drawn by KS

Comments: 3-State Buffer w/ Active High En

Title: XC4000 Family BUFE Macro
Comments: 3-State Buffer w/ Active High En
Date: 3rd March 1993
Sheet Size: A
Rev: A
Ver: 1
XC4000 Family OBUFE Macro

3-State Output Buffer with Active High Enable

22nd February 1993

Title: XC4000 Family OBUFE Macro
Comments: 3-State Output Buffer with Active High Enable
Date: 22nd February 1993
Sheet Size: A
Rev: A
XC4000 Family BUFE Macro

Comments: 3-State Buffer w/ Active High En

Date: 3rd March 1993

Sheet Size: A

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Copyright (c) 1993, Xilinx Inc.
XC4000 Family OBUFE Macro

Comments: 3-State Output Buffer with Active High Enable

Date: 22nd February 1993

Copyright (c) 1993, Xilinx Inc.
XC4000 Family BUFE Macro

3-State Buffer w/ Active High En

Date: 3rd March 1993
Sheet Size: A
Rev: A

Comments: 3-State Buffer w/ Active High En
XC4000 Family OBUFE Macro

3-State Output Buffer with
Active High Enable

Date: 22nd February 1993
Copyright (c) 1993, Xilinx Inc.

drawn by KS
Title: XC4000 Family OBUFE Macro
Comments: 3-State Output Buffer with
Active High Enable
Date: 22nd February 1993
Sheet Size: A
Rev: A
D Flip-Flop
XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.
drawn by KS
Sheet Size: A

Comments: D Flip-Flop
Rev: A

Title: XC4000 Family FD Macro
Date: 23rd December 1992
Sheet Size: A
D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Copyright (c) 1993, Xilinx Inc.

Sheet Size: A
Rev: A
Version: 1

Drawn by KS
Date: 14th December 1992
2-to-1 Multiplexer

D0

S0

D1

AND2B1

AND2

OR2

O
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.
XC4000 Family M2_1 Macro

2-to-1 Multiplexer

drawn by KS
Copyright (c) 1993, Xilinx Inc.

Date: 14th December 1992
Sheet Size: A
Rev: A
Ver: 1
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992

Sheet Size: A

Rev: A

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A

Copyright (c) 1993, Xilinx Inc.
XC4000 Family M2_1 Macro

2-to-1 Multiplexer

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A

D0
S0
D1
M0
AND2B1
M1
AND2
OR2
O
XC4000 Family M2_1 Macro

2-to-1 Multiplexer

drawn by KS
Copyright (c) 1993, Xilinx Inc.

Title: XC4000 Family M2_1 Macro

Comments: 2-to-1 Multiplexer

Date: 14th December 1992

Sheet Size: A
Rev: A
Ver: 1
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Comments: drawn by KS
Copyright (c) 1993, Xilinx Inc.

Sheet Size: A
Rev: A

Date: 14th December 1992
Ver: 1
2-to-1 Multiplexer

- M0
- M1
- O
- D0
- S0
- D1
- AND2B1
- AND2
- OR2

XC4000 Family M2_1 Macro

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Sheet Size: A

Rev: A

Ver: 1
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer
Comments: 
Date: 14th December 1992
Sheet Size: A

D0 -> M0
S0 -> AND2B1
D1 -> M1
AND2
OR2 -> O

drawn by KS
Copyright (c) 1993, Xilinx Inc.
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992

Sheet Size: A

Rev: A

Copyright (c) 1993, Xilinx Inc.
drawn by KS

D0
S0
D1

AND2B1

M0
AND2

M1

OR2

O
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A
XC4000 Family M2_1 Macro
2-to-1 Multiplexer

D0
M0
AND2B1
S0
AND2
D1
M1
OR2
O
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Comments: 2-to-1 Multiplexer

Date: 14th December 1992

Sheet Size: A

Rev: A
XC4000 Family M2_1 Macro

2-to-1 Multiplexer

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.
2-to-1 Multiplexer

Inputs:
- D0
- S0
- D1

Outputs:
- M0
- M1
- O

Logic gates:
- AND2B1
- OR2

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Copyright (c) 1993, Xilinx Inc.
XC4000 Family M2_1 Macro

2-to-1 Multiplexer

drawn by KS
Copyright (c) 1993, Xilinx Inc.

XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A
Ver: 1
XC4000 Family M2_1 Macro

2-to-1 Multiplexer

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A
Ver: 1

Copyright (c) 1993, Xilinx Inc.
drawn by KS

D0
M0
S0
AND2B1
M1
D1
AND2
OR2
O
2-to-1 Multiplexer

- D0
- D1
- S0
- AND2
- AND2B1
- M0
- M1
- OR2
- O
XC4000 Family M2_1 Macro
2-to-1 Multiplexer

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Ver: 1
Rev: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.
2-to-1 Multiplexer with Enable

Title: XC4000 Family M2_1E Macro
Comments: 2-to-1 Multiplexer with Enable
Date: 16th December 1992
Sheet Size: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.
FDCE

VCC

D CE Q

C CLR

GND

RLOC=R0C0

D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Sheet Size: A

Ver: 1

Rev: A
2-to-1 Multiplexer

D0

S0

D1

AND2

M1

AND2B1

M0

OR2

O
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992
Sheet Size: A

Copyright (c) 1993, Xilinx Inc.
XC4000 Family M2_1 Macro

2-to-1 Multiplexer
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992

Copyright (c) 1993, Xilinx Inc.
drawn by KS

Sheet Size: A
Rev: A
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A
Sheet Size: A
Rev: 1
Ver: 1

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A

And2B1

Or2

D0

S0

D1

M0

M1

O
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A

D0
S0
D1
M0
M1
O
AND2B1
AND2
OR2

Copyright (c) 1993, Xilinx Inc.
drawn by KS
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A
Ver: 1
2-to-1 Multiplexer

Input:
- D0
- S0
- D1

Intermediate:
- AND2B1
- AND2

Output:
- OR2
- O

Logic Diagram:
AND2B1: M0
AND2: M1
OR2: O

Characteristics:
- XC4000 Family M2_1 Macro
- 2-to-1 Multiplexer

Details:
- Title: XC4000 Family M2_1 Macro
- Comments: 2-to-1 Multiplexer
- Date: 14th December 1992
- Sheet Size: A
- Rev: A
- Copyright (c) 1993, Xilinx Inc.
AND2B1

OR2

AND2

Sheet Size: A

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A

Copyright (c) 1993, Xilinx Inc.
drawn by KS
Copyright (c) 1993, Xilinx Inc.
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A

The diagram represents a 2-to-1 multiplexer with inputs D0, D1, S0, and outputs M0, M1, O. The 2-to-1 multiplexer selects between inputs D0 and D1 based on the select line S0.
XC4000 Family M2_1 Macro

2-to-1 Multiplexer

drawn by KS
Copyright (c) 1993, Xilinx Inc.

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A
XC4000 Family M2_1 Macro

2-to-1 Multiplexer

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A

Copyright (c) 1993, Xilinx Inc.
drawn by KS

D0
S0
D1

AND2B1
AND2

M0
M1
S0

OR2

O
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992

Sheet Size: A

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer

Date: 14th December 1992

Sheet Size: A

Copyright (c) 1993, Xilinx Inc.

drawn by KS
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992

Sheet Size: A

Rev: A

Copyright (c) 1993, Xilinx Inc.
drawn by KS

D0 → AND2B1 → M0 → OR2 → O

S0 → AND2B1 → M0

D1 → AND2 → M1 → OR2 → O
XC4000 Family M2_1 Macro

2-to-1 Multiplexer

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A
Ver: 1
A 3 2 1
B

Sheet Size: A
Rev: 1
Ver: A
Comments: 2-to-1 Multiplexer

Title: XC4000 Family M2_1 Macro
Date: 14th December 1992

Copyright (c) 1993, Xilinx Inc.

drawn by KS, Xilinx Inc.

D0
S0
D1

AND2
AND2B1
M2
M0
M1
OR2

O
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: 1

2-to-1 Multiplexer Circuit Diagram
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: 1

D0
S0
D1
M0
M1
AND2B1
AND2
OR2
O

Copyright (c) 1993, Xilinx Inc.
drawn by KS

XILINX
2-to-1 Multiplexer with Enable

Drawn by KS
Copyright (c) 1993, Xilinx Inc.

Title: XC4000 Family M2_1E Macro
Comments: 2-to-1 Multiplexer with Enable
Date: 16th December 1992
Sheet Size: A
D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.
drawn by KS

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A

Ver: 1
Rev: A
D Flip-Flop
XC4000 Family FD Macro

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A
Rev: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.
Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A
D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Title: XC4000 Family FD Macro
Comments: D Flip-Flop

Date: 23rd December 1992
Sheet Size: A

Ver: 1
Rev: A
XC4000 Family M2_1 Macro
2-to-1 Multiplexer

Date: 14th December 1992
Sheet Size: A
Rev: A

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Copyright (c) 1993, Xilinx Inc.
2-to-1 Multiplexer

Inputs:
- D0
- D1
- S0

Logic Gates:
- AND2B1
- AND2
- OR2
- M0
- M1
- C

Output:
- O
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992

D0 → AND2B1 → OR2 → O

S0 → ANDB1

D1 → AND2

M0 → OR2

M1 → OR2

drawn by KS
Copyright (c) 1993, Xilinx Inc.
XC4000 Family M2_1 Macro
2-to-1 Multiplexer

Title:  XC4000 Family M2_1 Macro
Comments:  2-to-1 Multiplexer
Date:  14th December 1992
Sheet Size:  A
Rev:  A
Ver:  1

Copyright (c) 1993, Xilinx Inc.
drawn by KS

D0
S0
D1
AND2B1
M0
AND2
M1
OR2
O
XC4000 Family M2_1 Macro

2-to-1 Multiplexer

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer

Date: 14th December 1992
Sheet Size: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.
XC4000 Family M2_1 Macro

2-to-1 Multiplexer
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A

D0
S0
D1

AND2B1
M0
M1

OR2
O

drawn by KS
Copyright (c) 1993, Xilinx Inc.
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.

D0 -> AND2B1 -> O
S0 -> AND2B1 -> M0
D1 -> AND2 -> M1
M0 -> OR2 -> O
M1 -> OR2 -> O
XC4000 Family M2_1 Macro

2-to-1 Multiplexer

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A

D0 -> AND2B1
S0 -> M0
D1 -> AND2

AND2B1 -> OR2
O
XC4000 Family M2_1 Macro
2-to-1 Multiplexer

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A
Ver: 1
The diagram represents a 2-to-1 multiplexer. It consists of two AND gates, AND1 and AND2, and two OR gates, OR1 and OR2. The inputs are labeled D0, D1, S0. The output is labeled O. The diagram shows the connections between these components.
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer
Comments: 
Date: 14th December 1992
Sheet Size: A
Ver: 1
Rev: A

Copyright (c) 1993, Xilinx Inc.
drawn by KS
2-to-1 Multiplexer

D0
S0
D1

AND2B1
AND2

M0
M1

OR2

O
FDCE

D  Q
CE  Q
CLR

RLOC=R0C0

VCC

GND

D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A
D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Title:XC4000 Family FD Macro
Comments:D Flip-Flop
Date:23rd December 1992
Sheet Size:A
XC4000 Family M2_1 Macro

2-to-1 Multiplexer

drawn by KS
Copyright (c) 1993, Xilinx Inc.

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A

D0

S0

D1

AND2B1

M0

AND2

M1

OR2

O
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A

AND2 \( \rightarrow \) OR2
AND2B1
M0
S0
D0
M1
D1
O
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer

Date: 14th December 1992
Sheet Size: A

Copyright (c) 1993, Xilinx Inc.

drawn by KS

2-to-1 Multiplexer Diagram

- Inputs: D0, D1, S0
- Outputs: M0, M1, O
- Logic Gates: AND2, AND2B1, OR2
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992
Ver: 1
Sheet Size: A
Rev: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A
2-to-1 Multiplexer

- **D0**
- **S0**
- **D1**
- **AND2**
- **M0**
- **M1**
- **AND2B1**
- **OR2**
- **O**

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A
Ver: 1

Copyright (c) 1993, Xilinx Inc.

drawn by KS

XILINX
XC4000 Family M2_1 Macro
2-to-1 Multiplexer

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A
Ver: 1

drawn by KS
Copyright (c) 1993, Xilinx Inc.
2-to-1 Multiplexer

D0
S0
D1

AND2B1
AND2

M0
M1

OR2

O
XC4000 Family M2_1 Macro

2-to-1 Multiplexer

D0
S0
D1
M0
M1
S0
AND2B1
AND2
OR2
O

Copyright (c) 1993, Xilinx Inc.
drawn by KS
Date: 14th December 1992
Sheet Size: A
2-to-1 Multiplexer

D0
S0
D1

AND2
AND2B1
M0
M1
OR2
O
AND2B1

OR2

AND2

Sheet Size: A

Rev: 1

Ver: A

Title: XC4000 Family M2_1 Macro

Comments: 2-to-1 Multiplexer

Date: 14th December 1992

Sheet Size: A

Rev: A

Copyright (c) 1993, Xilinx Inc.

drawn by KS

XILINX

1

2

3

4

1

2

3

4

A

B

A

B
FDCE

VCC

D

Q

CE

C

CLR

RLOC=R0C0

GND

D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.
drawn by KS

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A
Rev: A
D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992
Sheet Size: A

Copyright (c) 1993, Xilinx Inc.

drawn by KS

14th December 1992
XC4000 Family M2_1 Macro

2-to-1 Multiplexer

Copyright (c) 1993, Xilinx Inc.

Drawn by KS
14th December 1992
XC4000 Family M2_1 Macro

2-to-1 Multiplexer

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: 1
Ver: A

Copyright (c) 1993, Xilinx Inc.
drawn by KS
14th December 1992
XC4000 Family M2_1 Macro
2-to-1 Multiplexer

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
2-to-1 Multiplexer

D0
S0
D1
M0
M1
O

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A
Ver: 1
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Comments: 2-to-1 Multiplexer

Date: 14th December 1992

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Copyright (c) 1993, Xilinx Inc.
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Comments: 2-to-1 Multiplexer

Date: 14th December 1992

Sheet Size: A

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Copyright (c) 1993, Xilinx Inc.
AND2 → OR2

D0 → AND2B1

S0 → AND2B1

D1 → AND2B1

M0 → OR2

M1 → OR2

O
XC4000 Family M2_1 Macro

2-to-1 Multiplexer

drawn by KS
Copyright (c) 1993, Xilinx Inc.

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A

Copyright (c) 1993, Xilinx Inc.
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Comments: 14th December 1992

Copyright (c) 1993, Xilinx Inc.

drawn by KS

Sheet Size: A

Rev: A
2-to-1 Multiplexer

D0
S0
D1

M0
M1
S0
OR2
AND2
AND2B1

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A

Copyright (c) 1993, Xilinx Inc.
drawn by KS
14th December 1992
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Copyright (c) 1993, Xilinx Inc.

Sheet Size: A
Rev: A
Ver: 1

Diagram Description:
- AND2B1 and AND2 are connected to M0 and M1, respectively.
- OR2 combines M0 and M1, producing the output O.
- D0, S0, and D1 are input signals to AND2B1, AND2, and OR2, respectively.
- The schematic represents a 2-to-1 multiplexer circuit in the XC4000 Family.
2-to-1 Multiplexer

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A
Ver: 1

Copyright (c) 1993, Xilinx Inc.
drawn by KS
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992

Sheet Size: A

Rev: A

Copyright (c) 1993, Xilinx Inc.

drawn by KS

14th December 1992
2-to-1 Multiplexer

D0 → M0
S0 → M0
D1 → M1

M0 → OR2
M1 → OR2

OR2 → O
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992

Sheet Size: A

Rev: A

Copyright (c) 1993, Xilinx Inc.
drawn by KS
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A

D0
S0
D1

AND2
M0
M1
AND2B1
OR2

O
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992

Sheet Size: A

Drawn by KS
Copyright (c) 1993, Xilinx Inc.

D0 → AND2 → O
S0 → AND2B1 → OR2 → O
D1 → AND2 → OR2 → O
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: 1
Ver: A
XC4000 Family M2_1 Macro

2-to-1 Multiplexer
AND2B1

OR2

AND2
D Flip-Flop

XC4000 Family FD Macro

23rd December 1992

Copyright (c) 1993, Xilinx Inc.
drawn by KS

Title: XC4000 Family FD Macro
Comments: D Flip-Flop
Date: 23rd December 1992
Sheet Size: A
Ver: 1
Rev: A
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer

Copyright (c) 1993, Xilinx Inc.
drawn by KS
14th December 1992
Sheet Size: A
Rev: A
Ver: 1

D0 → AND2B1 → M0 → OR2 → O
S0 → AND2B1 → M1 → OR2 → O
D1 → AND2 → M0 → OR2 → O
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992

Sheet Size: A

Rev: A
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992
Sheet Size: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992
Sheet Size: A

drawn by KS
Copyright (c) 1993, Xilinx Inc.
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992

Copyright (c) 1993, Xilinx Inc.
drawn by KS
Sheet Size: A
Rev: A
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A

```
D0 -- AND2B1 -- M0
S0 -- AND2B1 -- M1
D1 -- AND2B1 -- OR2

O
```

Copyright (c) 1993, Xilinx Inc.
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992

Sheet Size: A

Rev: A

Copyright (c) 1993, Xilinx Inc.
2-to-1 Multiplexer

D0
S0
D1

AND2

AND2B1

M0

OR2

M1

O

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Copyright (c) 1993, Xilinx Inc.

drawn by KS
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer

D0
S0
D1
M0
M1
AND2B1
AND2

O
OR2
XC4000 Family M2_1 Macro

2-to-1 Multiplexer

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Copyright (c) 1993, Xilinx Inc.

drawn by KS
Copyright (c) 1993, Xilinx Inc.
XC4000 Family M2_1 Macro

2-to-1 Multiplexer

Date: 14th December 1992

Sheet Size: A
Rev: A

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer

Copyright (c) 1993, Xilinx Inc.
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992

Sheet Size: A

Rev: A

Copyright (c) 1993, Xilinx Inc.

drawn by KS
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992

Sheet Size: A

Copyright (c) 1993, Xilinx Inc.
XC4000 Family M2_1 Macro
2-to-1 Multiplexer
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A

D0
S0
D1

AND2

M0

AND2B1

M1

OR2

O
XC4000 Family M2_1 Macro

2-to-1 Multiplexer

Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A

Copyright (c) 1993, Xilinx Inc.
Title:  XC4000 Family M2_1 Macro
Comments:  2-to-1 Multiplexer
Date:  14th December 1992
Sheet Size:  A
Rev:  A

drawn by KS
Copyright (c) 1993, Xilinx Inc.

D0
S0
D1

M0
AND2B1

M1
AND2

OR2
O
XC4000 Family M2_1 Macro

Title: 2-to-1 Multiplexer

Date: 14th December 1992

Copyright (c) 1993, Xilinx Inc.
Title: XC4000 Family M2_1 Macro
Comments: 2-to-1 Multiplexer
Date: 14th December 1992
Sheet Size: A
Rev: A
Ver: 1

D0
AND2
M1
OR2
O
S0
AND2B1
M0
D1
AND2

OR2

AND2B1

D0

S0

D1

O
2-to-1 Multiplexer with Enable

D0 -> AND3B1 (M0) -> OR2 (O)
E -> AND3B1 (M0)
S0 -> AND3B1 (M1)
D1 -> AND3

Title: XC4000 Family M2_1E Macro
Comments: 2-to-1 Multiplexer with Enable
Date: 16th December 1992
Sheet Size: A
Rev: A
Title: XC4000 Family M2_1E Macro
Comments: 2-to-1 Multiplexer with Enable
Date: 16th December 1992
Sheet Size: A
Rev: A